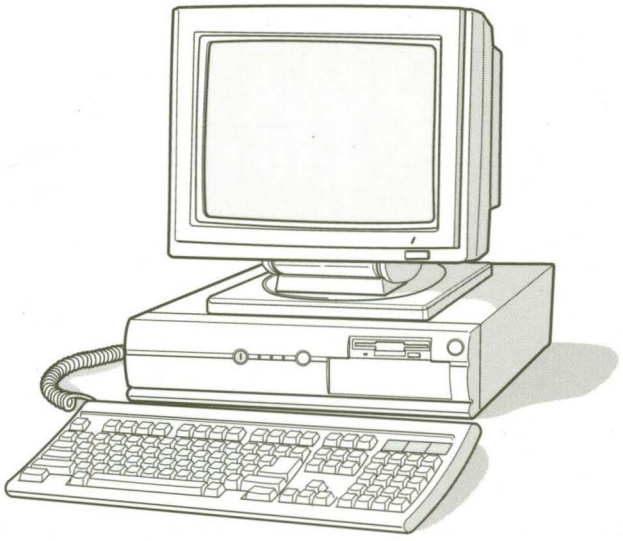
Service Manual

DeskMaster 486Q
(SD925E)



SAMSUNG

TRADE MARKS

MS-DOS and Windows are registered trademarks of Microsoft Inc.
IBM, Personal System/2 and PS/2 are registered trademarks of International Business Machines Corporation.
Intel 486SX, 487SX, 486DX, 486DX2 are registered trademarks of Intel Corporation.
SiS85C460 is registered trademarks of Silicon Integrated Systems Corporation.
CIRRUS GD-540X, GD-542X is registered trademarks of Cirrus Logic, Inc.

NOTICE : The information contained in this manual is subject to change without notice. No responsibility is assumed for errors or omissions in this document.

Copyright notice

Copyright (C) 1993, SAMSUNG Electronics Co., Ltd. All rights reserved.
This manual is copyrighted with all rights reserved. This manual may not be copied, in whole or in part, without consent of SAMSUNG. SAMSUNG reserves the rights to change, without notice, the specifications contained in this manual.

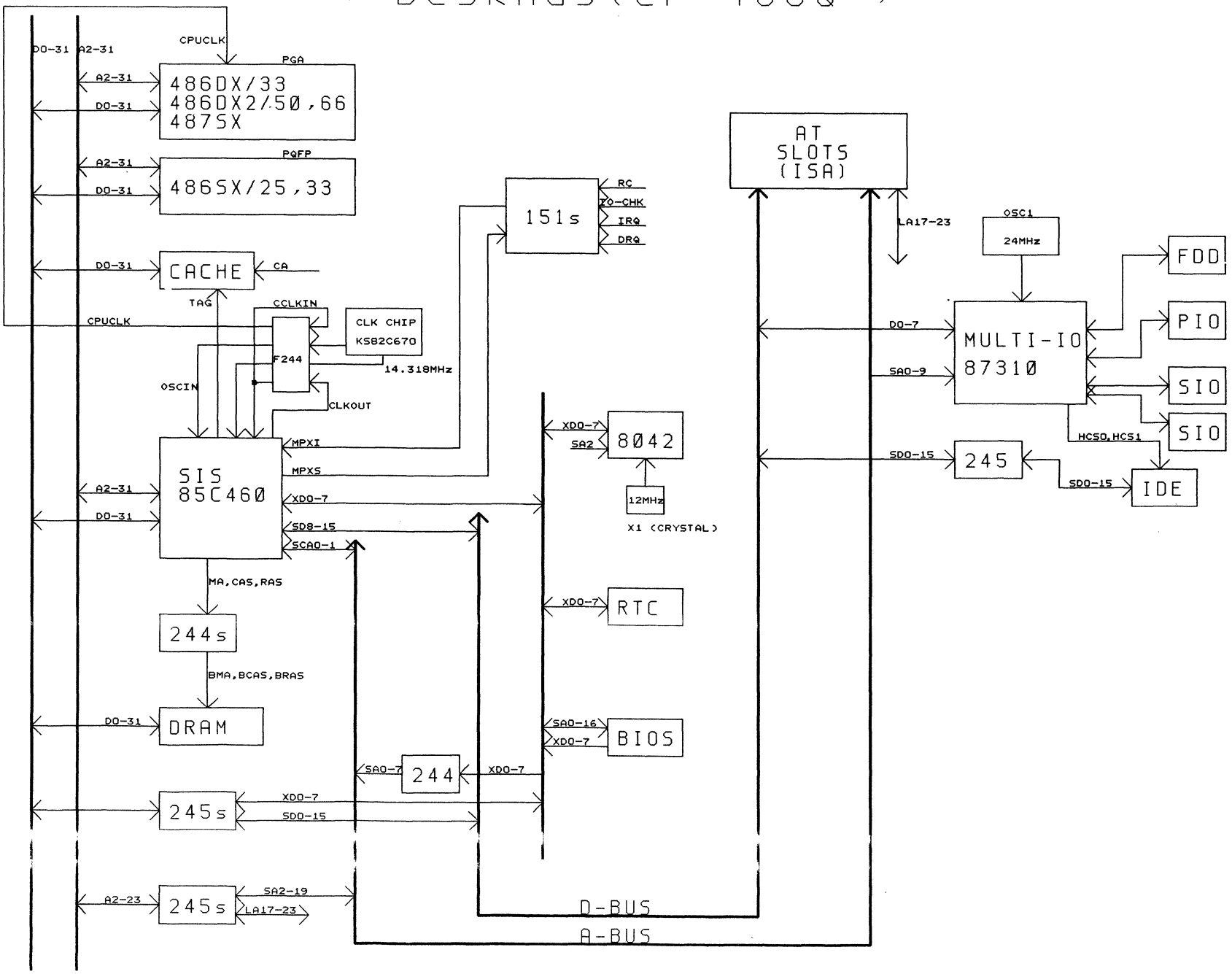
First Edition
Printed in KOREA

Table of Contents

Chapter 1. Overview

System Block Diagram
System Configuration
Power Supply
Exploded View
Mechanical Parts List

System Block Diagram



System Configuration

1. System Main Board

* CPU :	80486SX-25/33 Upgradable 80486DX-33, 80486DX2-50/66, 80487SX
* RAM :	Minimum 4MB, expandable up to 36MB using 1MB or 4MB SIMMs in the 8 SIMM sockets Required Access Time (70ns)
* Cache Memory (Option) :	32KB / 128KB
* ROM :	128KB EPROM
* Built-in I/O interface logics :	FDD interface logic, IDE interface logic
* Port :	1 Parallel Port(25-pin female), 2 Serial Port(9-pin male), PS/2 Mouse/Keyboard(6-pin Mini Din-Jack), 1 Video Port
* Video Board :	Built-in Local Super VGA 1280 x 1024 x 16 colors or 1024 x 768 x 256 colors or 800 x 600 x 64K colors or 640 x 480 x 16M colors with 1MB Video RAM
* Video RAM :	Basic 512KB, Up To 1MB
* Slot :	3 Expansion AT-Slots

2. Peripherals

* Keyboard :	IBM AT Compatible 101/102 key
* Mouse (Option) :	PS/2 Type
* FDD :	3.5-inch 1.44MB, 5.25-inch 1.2MB&360KB (Option)
* HDD (Option) :	3.5-inch

3. Power Supply

* Model :	PS-103, PS-103C
* Wattage :	100W

4. Cabinet

* Size :	Width(395mm), Depth(393mm), Height(98mm)
* Bay :	2 Open for 1 5.25-inch and 1 3.5-inch FDD, 1 Hidden for 1 3.5-inch HDD
* Front Panel :	Power/HDD/Turbo LED, Keylock Switch, Power/Reset Button
* Rear Panel :	Keyboard/Mouse/two Serial/parallel/Video Port, Power Inlet/Outlet, three Expansion Brackets

5. Softwares

* MS-DOS
* MS-Windows
* System Utilities
* VGA Utilities

Power Supply

The Power supply provides power for all of the option cards installed in the system unit, main board, floppy disk drive, hard disk drive, and keyboard.

1. Functional Description

1-1. Input Requirements

The power supply is able to operate at the frequency of either 50Hz or 60Hz and also can run at 90V to 132V, or 180V to 264V AC single phage.

1-2. Peak Inrush Current

The inrush current shall be less than the maximum current of its critical components (including power switch, fuse, bulk rectifiers, and the surge limiting device) for all conditions of line voltage.

1-3. Output Characteristics

1-4. Voltage Adjustment

Output Voltage	Wire Color	Tolerance(Accuracy)	Load Current(MIN-MAX)
+ 5V DC	Red	-5%, +5%	1.5A - 13.0A
+ 12V DC	Yellow	-5%, +5%	0.2A - 2.5A
- 12V DC	Brown	-10%, +10%	OA - 0.3A
- 5V DC	Blue	-10%, +10%	OA - 0.1A

+5V DC output is adjustable from 4.75V DC to 5.25V DC. The +5V DC output at the power supply output connector should be adjusted to between 4.9V DC and 5.1V DC by the manufacturer for typical load operation.

1-5. Over Voltage Protection

This feature is only for the +5V DC output. If a overvoltage fault occurs (internal to the power supply), the power supply shall shutdown before +5V DC and +12V DC output exceeds 130% of its maximum value.

1-6. Over Current protection

This feature is applied to the two outputs, +5V DC and +12V DC. If the load current of its output exceeds maximum values, 13A to 20A on the 5V DC and 5A to 8A on the 12V DC, the power supply shall shutdown and cause no damage to the system.

1-7. Short Circuit Protection

A short curcuit placed on any DC output (between outputs or between an output and DC return). If any short condition occurs, it shall cause no damage to the power supply or the system attached to the power supply.

2. Pin Assignments

2-1. Power Connector for Main Board

Pin No.	Color	Voltage(Vdc)
1	Yelow	+12Vdc
2	Brown	-12Vdc
3-6	Black	GND(return)
7	Blue	-5Vdc
8-10	Red	+5Vdc

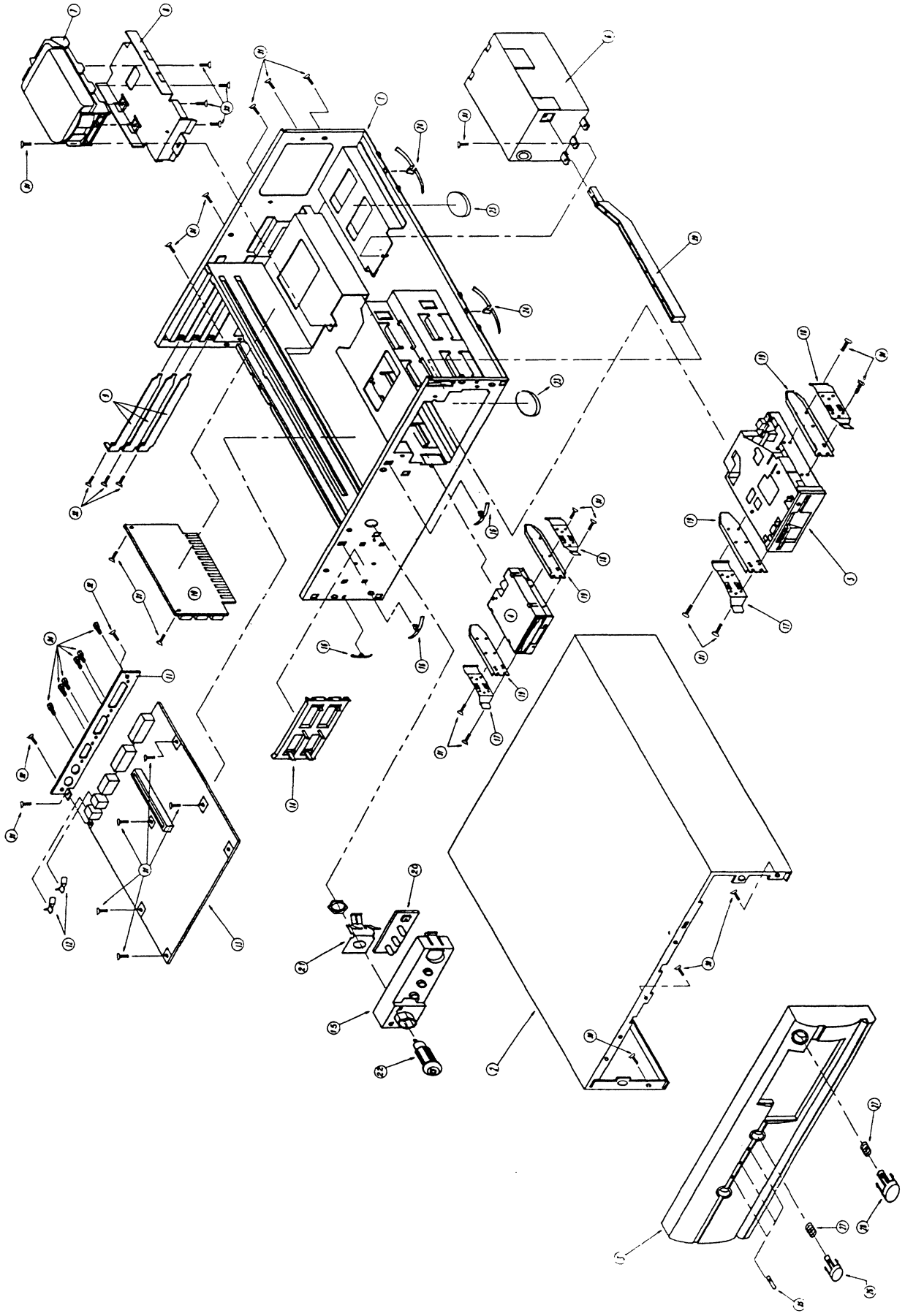
2-2. Power Connector for 3.5-inch FDD

Pin No.	Color	Voltage(Vdc)
1	Red	+5Vdc
2	Black	GND(return)
3	Black	GND(return)
4	Yellow	+12Vdc

2-3. Power Connector for 5.25-inch FDD or HDD

Pin No.	Color	Voltage(Vdc)
1	Yellow	+12Vdc
2	Black	GND(return)
3	Black	GND(return)
4	Red	+5Vdc

Exploded View



Mechanical Parts List

NO	DESCRIPTION	PART NUMBER	SPECIFICATION	Q'TY
1	BOTTOM-ASS'Y	98901-902-110	EGI	1
2	CHASSIS-COVER	96121-907-210	EGI T1.0	1
3	BEZEL-ASS'Y	98901-902-310	ABS 94Vo	1
4	FDD 3.5" 1.44M			1
5	FDD 95TPI			1
6	SMPS-ASS'Y			1
7	HDD 3.5"			1
8	BRKT-HDD BASE	96612-920-110	EGI T1.0	1
9	BRKT-BLANK	98424-971-820	SPC-1 T1.0 NI	3
10	BUS-BOARD			1
11	BRKT-CONNECTOR'B	96613-920-412	EGI T1.0	1
12	CONTACT-KBD	96674-906-611		2
13	MOTHER-BOARD			1
14	GUIDE-PCB	96043-900-910	P.C. BLACK	1
15	PANEL-CONTROL	97603-900-910	ABS 94Vo	1
16	BRKT-CONTACT	96614-913-510	SUS-304 1/2H	3
17	SPRING-BRKT FDD(L)	96674-905-910		2
18	SPRING-BRKT FDD(R)	96674-905-920		2
19	BRKT-GUIDE FDD	96613-921-411	EGI T1.0	4
20	LED-PCB			1
21	SPRING KEY-LOCK	96674-908-110	SUS T0.2	1
22	KEY-LOCK			1
23	FOOT-RUBBER	98464-904-720	NATURAL-RUBBER	4
24	SPRING-CON COVER	96674-905-510	STS T0.3	4
25	LENS-LED	97654-901-611	ACRYL NATURAL	3
26	KNOB-RESET	97624-973-010	ABS 94Vo	1
27	SPRING-POWER	96674-902-010	SUS-WPA P10.5,ST-35	2
28	KNOB-POWER	97624-905-410	ABS 94Vo	1
29	LEVER-S/W	96613-919-410	ABS 94Vo	1
30	SCREW-TAPTITE, PH	97408-130-101	+B-3*10 FE FZY	3
31	SCREW-BH	97088-130-062	+M3*6 FE FZW	19
32	SCREW-TAPTITE, BH	97458-230-062	+S-3*6 FE FZY	5
33	SCREW-PH/RH	97044-900-310	UNC6-32*1/4,SM20C	4
34	SCREW-HEXAGON	97094-900-310	UNC4-40,SUM24L,FN2	6

Chapter 2. Diagnostics

System Error Messages
System Beep Codes
SSAD (SAMSUNG Advanced Diagnostics)
Main Logic Debugging Flow
Video Logic Debugging Flow
Power Supply Debugging Flow

System Error Messages

The Power-on Self Test (POST) is a diagnostic test that resides in the ROM BIOS and runs automatically whenever the system is turned on or reset. The POST checks and initializes the processor, the memory and the peripheral devices connected to the computer (keyboard, monitor, disk drives, etc.).

1. POST and Boot Messages

If the POST can display a message on the monitor screen, it will beep the speaker twice as the message appears. However, when an error occurs before the monitor is initialized, the POST cannot display messages on the screen. Therefore, it will instead sound a series of beeps.

POST may display a message during a normal test or when it encounters a non-fatal system-board failure or an off-board failure. The messages can indicate errors in hardware, software, or firmware, or they may be informational only.

The next three sections provide a general grouping of messages, with each group arranged in alphabetical order. Each message is accompanied by a short paragraph that describes the message and gives a recommended solution to the problem (if one is suspected to exist).

2. POST and Boot Error Messages

Message: Diskette drive 0 seek failure.
Possible cause: Drive A has either failed or is missing.
Solution: Check that drive A is present and the diskette is inserted properly. If they are, then drive A may have failed.

Message: Diskette drive 1 seek failure.
Possible cause: Drive B has either failed or is missing.
Solution: Check that drive B is present and that the diskette is inserted properly. If they are, then drive B may have failed.

Message: Diskette read failure - strike F1 to retry boot, F2 for setup utility.
Possible cause: The two most likely causes for this condition are: (1) the diskette is not bootable, and (2) the diskette is defective.
Solution: Replace the diskette with a bootable diskette and try again. Clean the drive heads, if necessary.

Message: Diskette subsystem reset failed.
Possible cause: The diskette adapter cable has failed.
Solution: Check the diskette adapter cable.

Message: Display adapter failed; using alternative.
Possible cause: The monitor type jumpers are set incorrectly or the primary video adapter failed.

Solution: Check to ensure that the monitor jumper type is set correctly. Check the primary video adapter.

〈 NOTE 〉

The following basic message precedes any of the possible errors numbered 1 through 6. These errors can only occur when the setup program is run.

Message: Errors have been found during the power-on self test in your computer.
The errors were:
1. Clock chip lost power
2. CMOS checksum invalid
3. Incorrect configuration data in CMOS
4. Memory size in CMOS invalid
5. Disk C: failed initialization
6. Time or Date in CMOS is invalid
Hit any key to continue

Possible cause: The configuration information stored in the real-time clock chip does not agree with the hardware configuration of your system.

Solution: Check that the jumper settings on the system board agree with the hardware configuration. Rerun the setup program and reenter data that could account for the indicated error.

Message: Gate A20 failure.
Possible cause: The computer cannot switch into the protected mode.
Solution: Call your service representative.

Message: Hard disk configuration error.
Possible cause: The specified configuration is incorrect.
Solution: Rerun the setup program and enter the correct hard disk drive type.

Message: Hard disk controller failure.
Possible cause: The hard disk controller card has failed.
Solution: Check both ends of the controller's cables and reseat the hard disk controller. If the message occurs again, replace the hard disk controller's cable.

Message: Hard disk failure.
Possible cause: The hard disk is defective
Solution: Check the system configuration and drive type and rerun the setup program. Check both ends of the controller's cable and reseat the hard disk controller. Check the hard drive jumper and termination resistor.

Message: Hard disk read failure - strike F1 to retry boot, F2 for setup utility.
Possible cause: The hard disk is defective.
Solution: Check the system configuration and drive type and rerun the setup program. Check both ends of the controller's cable.

Message: Hex-value Optional ROM bad checksum=hex-value

Possible cause: A peripheral card contains a defective ROM or its address conflicts with another card.
Solution: Replace the ROM or the peripheral card, or correct the address conflict.

Message: Invalid configuration information-please run SETUP program.
Possible cause: The memory size is incorrect, the display is configured incorrectly or the number of diskette drives is incorrect.
Solution: Check the system configuration and rerun the setup program.

Message: Keyboard clock line failure.
Possible cause: Either the keyboard or the keyboard cable connection is defective.
Solution: Call your service representative.

Message: Keyboard data line failure.
Possible cause: Either the keyboard or the keyboard cable connection is defective.
Solution: Check the keyboard connection. If the connection is good, the keyboard may have failed.

Message: Keyboard is locked - please unlock - Strike the F1 key to continue, F2 to run the setup utility.
Possible cause: The keyboard lock (located at the front of the computer) is activated.
Solution: Unlock the keyboard and try again.

Message: Keyboard stuck key failure
Possible cause: One or more of the keys is pressed.
Solution: Release the key or keys and try again.

Message: Memory address line failure at hex-value, read hex-value expecting hex-value.
Possible cause: One of the SIMMs or its associated circuitry has failed.
Solution: Check for a defective SIMM and replace it if necessary. If the message repeats, contact your service representative.

Message: Memory data line failure at hex-value, read hex-value, expecting hex-value.
Possible cause: One of the SIMMs or its associated circuitry has failed.
Solution: Check for a defective SIMM and replace it if necessary. If the message appears again, contact your service representative.

Message: Memory odd/even logic failure at hex-value, read hex value expecting hex-value.
Possible cause: One of the SIMMs or associated circuitry has failed.
Solution: Check for a defective SIMM and replace it if necessary. If the message appears again, contact your service representative.

Message: Memory parity failure at hex-value, read hex-value expecting hex-value.
Possible cause: One of the SIMMs or its associated circuitry has failed.
Solution: Check for a defective SIMM and replace it if necessary. If the message repeats, contact your service representative.

Message: Memory write/read failure at hex-value, read hex-value, expecting hex-value.

Possible cause: One of the SIMMs or associated circuitry has failed.
Solution: Check for a defective SIMM and replace it if necessary. If the message reappears, contact your service representative.

Message: No boot device available - strike F1 to retry boot, F2 for setup utility.
Possible cause: If booting from a diskette, the above message means that it is a non-bootable type or the diskette drive is defective. If booting from a hard disk, the message that it may not be formatted or that the disk drive is defective. The problem could also be in the disk controller board.
Solution: Make sure that diskette drive A contains an operating system diskette. If applicable, make sure the hard disk drive contains an operating system. Check the disk controller board.

Message: No boot sector on hard disk - strike F1 to retry boot, F2 for setup utility.
Possible cause: The hard disk is not formatted as a system disk.
Solution: Format the disk with the /S option.

Message: No timer tick interrupt.
Possible cause: The timer chip on the system board may have failed.
Solution: Contact your service representative.

Message: Not a boot diskette - strike F1 to retry boot, F2 for setup utility.
Possible cause: The diskette in drive A is not formatted as a system disk.
Solution: Replace the diskette with a bootable diskette and try again.

Message: Shutdown failure.
Possible cause: The keyboard controller or its associated logic has failed.
Solution: Call your service representative.

Message: Time-of-day not set - Please run the SETUP program.
Possible cause: The date and time information is not set in the real-time clock.
Solution: Run the setup program and set the date and time.

Message: Timer chip counter 2 failed.
Possible cause: The timer chip or the interrupt controller on the system board may have failed.
Solution: Contact your service representative.

Message: Unexpected interrupt in protected mode.
Possible cause: The system received an interrupt when in protected mode - probably while testing memory.
Solution: Contact your service representative.

3. POST and Boot Information Messages

Message: Hex-value Base Memory
Meaning: Indication of the amount of base memory that has been tested successfully.

Message: Hex-value extended

Meaning: Indication of the amount of extended memory that has been tested successfully.

Message: Decreasing available memory.
Meaning: This message immediately follows any memory error message, informing you that memory chips are failing. Check that each SIMM on the system board is installed correctly. If the memory error message reappears, contact your service representative.

Message: Memory test terminated by keystroke.
Meaning: The spacebar was pressed during the memory test. Reboot the system if you want to rerun the POST.

Message: Strike the F1 key to continue, F2 to run the setup utility.
Meaning: The POST detected an error prior to boot. Pressing the F1 key lets the computer try to boot. Pressing the F2 key runs the setup utility.

4. Run-Time Messages

Run-time messages are displayed if an error occurs after the boot process is complete.

Message: I/O card parity interrupt at address hex-value. Type (S)hut off NMI, (R)eboot, other keys to continue.
Possible cause: A peripheral card has failed.
Solution: Type S to shut off the nonmaskable interrupt (NMI). This will temporarily allow you to continue. Replace the peripheral card.

Message: Memory parity interrupt at address hex-value. Type (S)hut off NMI, (R)eboot, other keys to continue.
Possible cause: One or more memory chips have failed.
Solution: Type S to shut off the nonmaskable interrupt (NMI). This will temporarily allow you to continue. Check the seating of the SIMMs and replace any defective SIMM.

Message: Unexpected HW interrupt at address hex-value. Type (R)eboot, other keys to continue.
Possible cause: This could be any hardware-related problem.
Solution: Check the hardware or call your service representative.

Message: Unexpected SW interrupt at address hex-value. Type (R)eboot, other keys to continue.
Possible cause: There is an error in the software program.
Solution: Try turning the computer off and then on again. If that doesn't work, check the program.

System Beep Codes

If the POST finds an error and cannot display a message on the monitor, the POST issues a series of beeps to indicate the error and places a value in I/O port 80H.

For example, a failure of bit 3 in the first 64 KB of RAM is indicated by a 2-1-4 beep code (a burst of two beeps, a single beep, and a burst of four beeps). In addition, the POST writes a value to I/O port 80H to enable debugging tools to identify the area of failure.

Tables 1 and 2 list the beep codes and I/O port values that the POST generates when it encounters error conditions.

Table 1 lists fatal errors (errors that halt the system).
Table 2 lists the non-fatal errors (errors that aren't serious enough to halt the system). Both tables list other conditions that have no beep codes.

One beep code is not listed in Tables 1 or 2: a long beep followed by one or more short beeps indicates a video adapter failure. No beep code is sounded if a test is aborted while in progress.

Table 1. Beep Codes for Fatal Errors; and I/O Port Contents for Errors and Status

Beep Code	Description of Error	Contents of I/O Port 80H
2-1-1	Bit 0 1st 64 KB RAM failure	10H
2-1-2	Bit 1 1st 64 KB RAM failure	11H
2-1-3	Bit 2 1st 64 KB RAM failure	12H
2-1-4	Bit 3 1st 64 KB RAM failure	13H
2-2-1	Bit 4 1st 64 KB RAM failure	14H
2-2-2	Bit 5 1st 64 KB RAM failure	15H
2-2-3	Bit 6 1st 64 KB RAM failure	16H
2-3-4	Bit 7 1st 64 KB RAM failure	17H
2-3-1	Bit 8 1st 64 KB RAM failure	18H
2-3-2	Bit 9 1st 64 KB RAM failure	19H
2-3-3	Bit A 1st 64 KB RAM failure	1AH
2-3-4	Bit B 1st 64 KB RAM failure	1BH
2-4-1	Bit C 1st 64 KB RAM failure	1CH
2-4-2	Bit D 1st 64 KB RAM failure	1DH
2-4-3	Bit E 1st 64 KB RAM failure	1EH
2-4-4	Bit F 1st 64 KB RAM failure	1FH
3-1-1	Slave DMA register failure	20H
3-1-2	Master DMA register failure	21H
3-1-3	Master interrupt mask register failure	22H
3-1-4	Slave interrupt mask register failure	23H
None	Interrupt vector loading in progress	25H
3-2-4	Keyboard controller test failure	27H
None	Real-time clock power failure or checksum failure	28H

Table 2. Beep Codes for Non-Fatal Errors; and I/O Port Contents for Errors and Status

Beep Code	Description of Error	Contents of I/O Port 80H
None	80486 register test in progress	01H
1-1-3	Real-time clock write/read failure	02H
1-1-4	ROM BIOS checksum failure	03H
1-2-1	Programmable Interval Timer failure	04H
1-2-2	DMA initialization failure	05H
1-2-3	DMA page register write/read failure	06H
1-3-1	RAM refresh verification failure	08H
None	1st 64 KB RAM test in progress	09H
1-3-3	1st 64 KB RAM chip or data line failure multi-bit	0AH
1-3-4	1st 64 KB RAM odd/even logic failure	0BH
1-4-1	1st 64 KB RAM address line failure	0CH
1-4-2	1st 64 KB RAM parity test in progress or failure	0DH

SSAD (SAMSUNG Advanced Diagnostics)

1. What is SSAD(SAMSUNG Advanced Diagnostics) Program?

Welcome to the SSAD progrm. The diagnostic program is designed to the test on AT, 386 or 486 class PC. Since it is designed by module, you can test each hardware components individually. The diagnostic program is consist of several files. Those files are as following:

SSAD.EXE *SAUTO.INF* *SHELP.DAT* *ERROR.REC* *README.DOC*

SSAD.EXE --- The SSAD program file.
SAUTO.INF --- Auto test information file for the SSAD.
SHELP.DAT --- The help message file for the SSAD.
ERROR.REC --- The error record file for the SSAD.
README.DOC --- Documentation addendum for the SSAD.

2. How To Load The Diagnostic Program?

2.1. Preparation

Before the testing, you need the following things to test some area.

Math coprocessor	Needed to test coprocessor.
Blank Floppy Diskette	Needed when testing floppy drive.
SCSI LoopBack	Needed when testing SCSI loopback See Appendix A for diagram in loopback.
External Serial Loop-Back	Needed when testing serial port. See Appendix A for diagram in loopback.
External Parallel Loop-Back	Needed when testing parallel port. See Appendix A for diagram in loopback.
Parallel Printer	Needed when testing the printer.
Mouse	Needed when testing the mouse.

2.2. Installation

You may run the diagnostic program from the floppy disk directly or from the fixed disk. If you want to run it from the floppy diskette, insert the diagnostic program diskette to the floppy drive and load the program. If you want run from the fixed disk, create the directory for diagnostic program, copy all files from the diagnostic program diskette to the directory, and load the program from the fixed disk. When you run the diagnostic program from the floppy diskette, make sure you make backup copy of the diskette before running it.

2.3. Loading

1) From the drive that has the diagnostic program, type "SSAD" and pres [Enter]. Then the following screen will be displayed.

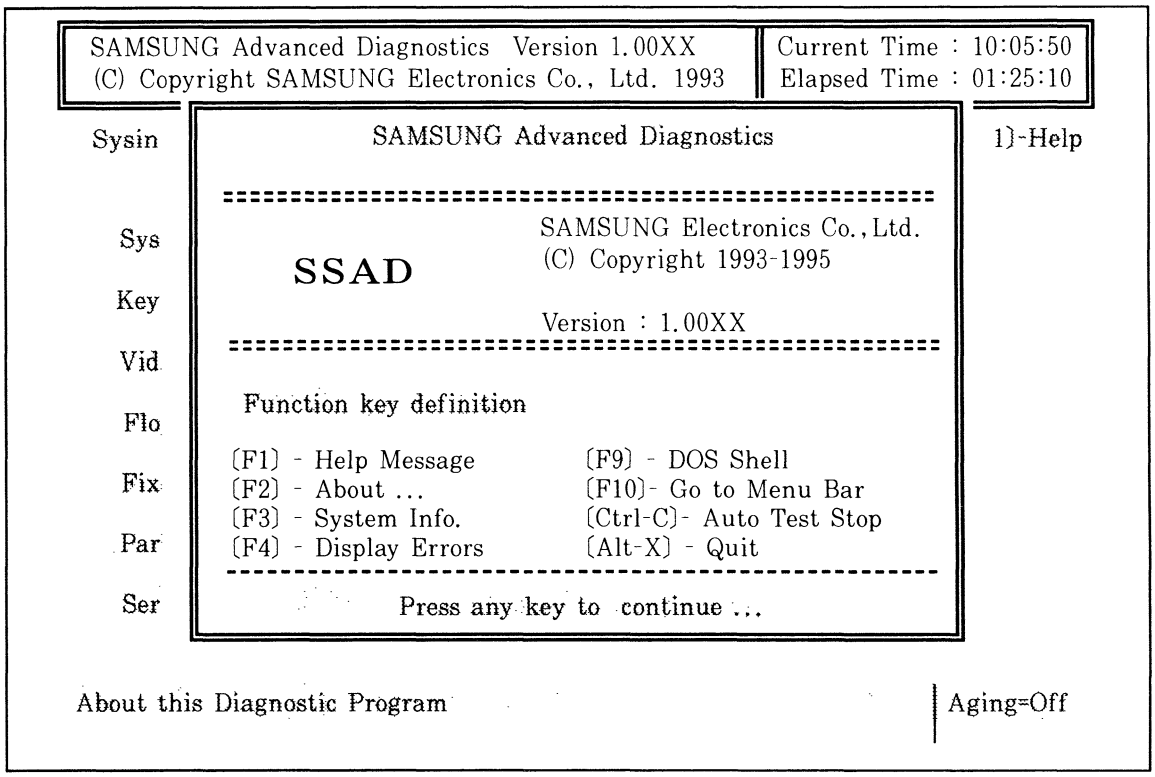


Figure 2.1 About and help message

2) Press any key to proceed to the next step. Now you are ready to run the SSAD program.

※ "SSAD" Option
C:\SSAD> SSAD /?

AT System Diagnostics. (C) Copyright SAMSUNG Electronics Co., Ltd. 1993

USE : SSAD [a(s|w) |nnn|] [/c |nnn|] [/f<file_name>] [/t |nn|] [/?]

<Command>
/as: Start string aging mode without keyin |aging test count|
/aw: Start week aging mode without keyin |aging test count|
/c : RAM test exchange loop count |odd number|
/f : Auto(Aging) test procedure file name <default:SAUTO.INF>
/t : Auto(Aging) mode terminal time |unit:hour|
/? : Help message

|nnn| : Decimal number

2.4. Main Menu and Selection

The following screen is the main menu of the diagnostic program.

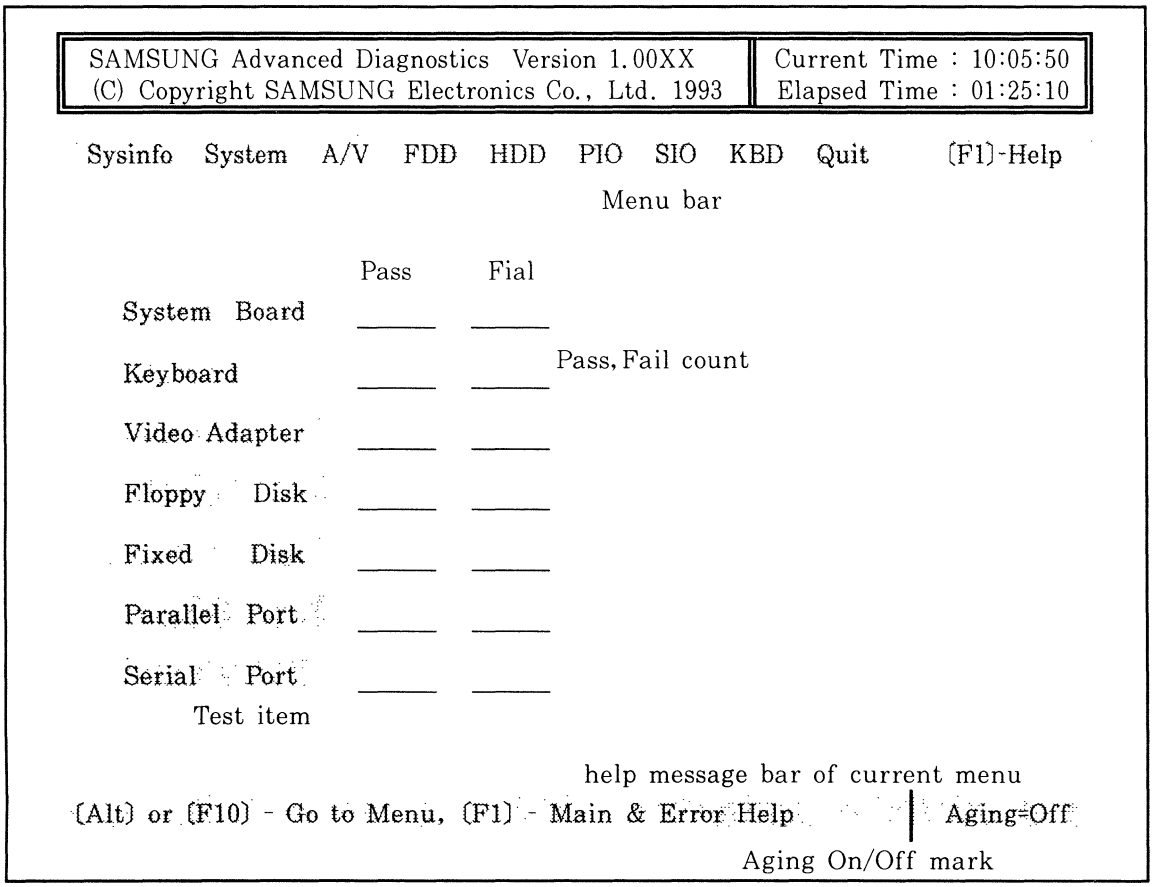


Figure 2.2 Main menu

1) The SSAD is a full-screen diagnostics, with pull-down menu support.
2) Display help message by pressing (F1) key.
3) You can start the manual test by pressing (F10) or (Alt) key.

3. Manual Test

This test should be performed by manually. You may run the test by module for each components of the system. When the test is failed, the error message will be display ask you if you save the error message. You may type "Y" to save or "N" not to save it.
If you press "Y", the error message will be stored in ERROR.REC file. The following screen will be displayed when you select System menu from the main menu.

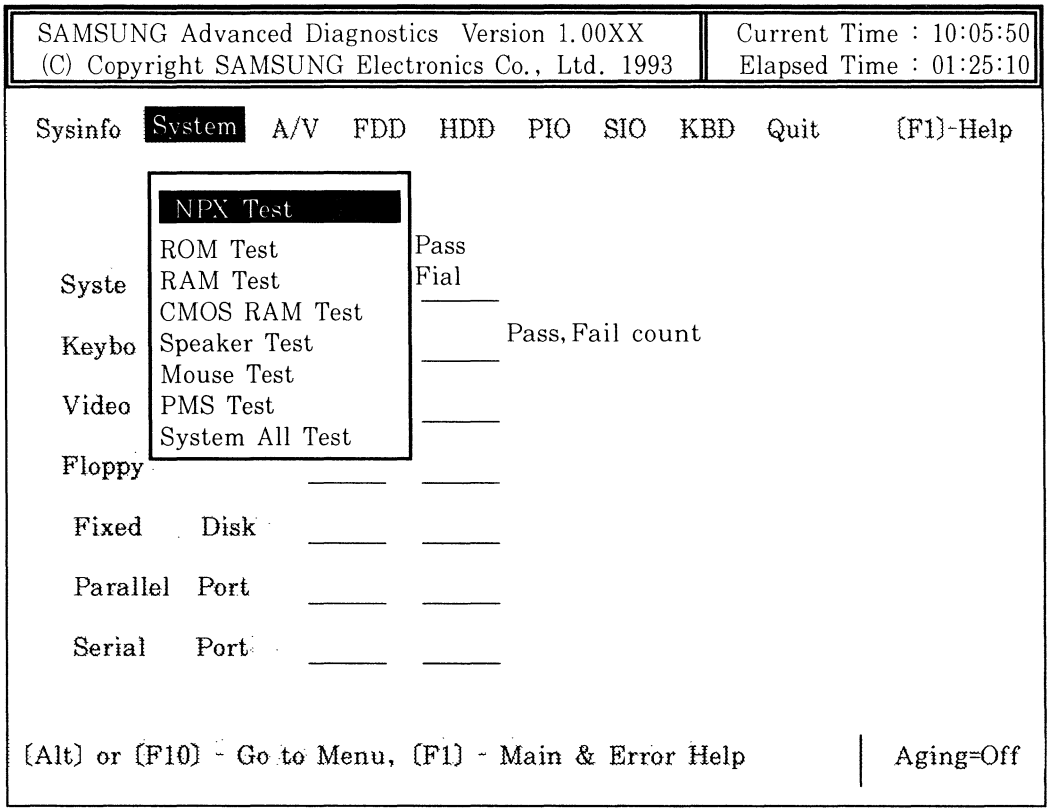


Figure 3.1 Selected menu

3.1. SysInfo Menu

1) System Configuration This function is selected, the following informations will be displayed on the center of the screen:

- ▶ DOS and EMS Version
- ▶ ROM BIOS Copyright
- ▶ CPU Type and Speed
- ▶ Coprocessor Type
- ▶ Base, Extended and Expanded Memory Sizes
- ▶ Diskette Drive and Fixed Disk Types
- ▶ Serial and Parallel Port Base Addresses
- ▶ Video Information
- ▶ Keyboard and Mouse Information

2) Display Test Errors
Display error message that have occurred during test. For each error the serial number, error code, description, date and time is displayed.

3) Init ERROR.REC
Initialize the ERROR.REC file, either by creation the file or removing all logged error.

4) Aging On/Off
Switching the aging On/Off menu.

5) Run All Test
Run all test in auto procedure file.

6) About ...
About this diagnostics.

3.2. System Menu

1) NPX Test
Test initialize, data transfer, status word, tag word, arithmetic, command, and exception if it is installed.

2) ROM Test
Test checksum of extended BIOS and system ROM modules.
The test range is (C000:0000 - D000:FFFF)

3) RAM Test
Test 640K base memory and extended memory up to 4GB.
You can cancel the program by using [Esc] key at any time.

4) CMOS RAM Test
Read/write test CMOS RAM(10H - 3FH). The current values of the CMOS RAM will be saved and restored after completing the test.

5) Speaker Test
Test the speaker sound at varying frequencies. You have to answer "Y" or "N" when the system asks you "Did the speaker respond correctly? (Y/N)" after completing the test.

6) Mouse Test
Test the mouse buttons and movement.
The mouse device driver should be installed before testing.

7) PMS Test
Test PMS(Power Management System) in Note PC.

8) A/V All Test
Continuously NPX, ROM, RAM, CMOS RAM, Speaker, Mouse and PMS test.

3.3. A/V Menu

1) Audio Card Test
Audio Card test.

2) Video Mode Test
Test all video modes with user confirmation.

3) Video Chip Test
Test EGA/VGA register, Video RAM, Read Mode 0/1, Write Mode 0/1/2, external palette RAM

3.4. FDD Menu

1) Reset Test
Reset the diskette drive controller and drive, forcing recalibration of the read/write heads. It tests and displays the status of the diskette surface.

2) Read/Write Test
Test read/write functions of the drive.

3) Seeking Test
Test sequential and random seek functions.

4) Motor Speed Test
Average the speed of the diskette drive over ten tries.
Average speed will be displayed as maximum and minimum speed with MSEC.

5) Format
Format the diskette. You have to select correct diskette.
After format, you may use the diskette as DOS formatted diskette.

6) FDD All Test
Continuously Reset, Read/Write, Seeking, and Motor Speed test.

3.5. HDD Menu

1) Reset Test
Test fixed disk controller and drive, forcing recalibration of the read/write heads.

2) R/W Test Test
Test read/write functions by saving the current track while testing.

3) Seeking Test
Test sequential and random seek functions of the fixed disk head.

4) Scanning Test
Scan the surface of the fixed disk and displays the error sector map.

5) SCSI Test Test
Test SCSI BIOS, ROM Checksum, control/status register, bus enable, loopback, interrupt on select enable bit.
You must attach the SCSI loopback connector before testing.
See Appendix A for diagram in loopback.

6) Format
Perform the low level format AT standard fixed disk.
You can input the factory bad sector map and interleave.

7) HDD All Test
Continuously Reset, Read/Write, Seeking, Scanning and SCSI loopback test.

3.6. PIO Menu

1) Loopback Test
Test internal and external loopback and interrupt line.
You must attach the PIO loopback connector before testing.
See Appendix A for diagram in loopback.

2) Printer Test
Test printing. You must have a printer attached.

3) PIO All Test
Continuously PIO loopback and Printer test.

3.7. SIO Menu

1) Internal Test
Test the serial port internally at 19200 and 2400 baud.
Test all the combination of baudrate, parity, data bits and stop bits.

2) External Test
Test the serial port externally at 19200, 9600, 1200 and 150 baud.
Test all the combination of baudrate, parity, data bits and stop bits.
You must attach the SIO loopback connector before testing.
See Appendix A for diagram in loopback.

3) Modem Test
Test of modem setup, baudrate, originate and answer mode carrier.

4) SIO All Test
Continuously SIO Internal, External and Modem test.

3.8. KBD Menu

1) Reset KBD Test
   Sends the reset command to the keyboard and varifies the return code.

2) KBDC BAT Test
   Test the keyboard controller.

3) Scan Code Test
   Test all the possible key scan code with user confirmation.
   The keyboard screen will be displayed and whenever you press the key, that key will be blinked on the keyboard. You have to make a decision if the keyboard works correctly. When finished the test, press [Esc] key twice to exit from the test. The program supports several different SSAD keyboard layout.

4) KBD All Test
   Continuously KBD Reset, KBDC BAT and Scan Code test.

3.9. Quit Menu

1) Exit to DOS
   This selection will exit the program and return to the DOS environment.
   You had better reboot the system before running additional software.

2) DOS shell
   This selection will invoke a DOS shell. Type 'exit' in the shell to return to the diagnostics.

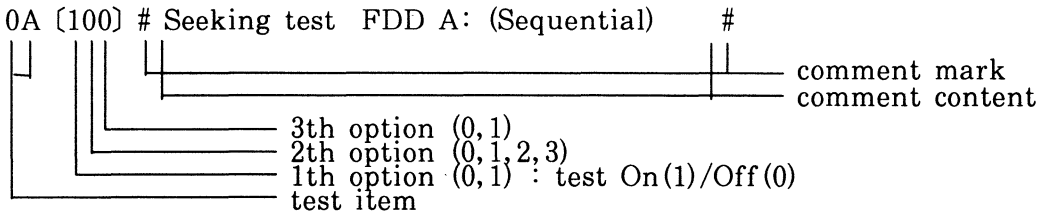
4. Automatic Test

4.1. Overview

The Automatic Test will be performed the test without any input from the user by the order that is defined in auto procedure(default: SAUTO.INF) file.

4.2. About of SAUTO.INF

1) SAUTO.INF file has information of auto test order for the SSAD.
This file format is as following:



① Test item --- Serial number of test item.
② 1th option --- Test On(1)/Off(1)
③ 2th option --- Test parameter of drive and port
④ 3th option --- Test Sequential(0)/Random(1)

2) You only modify 1th option in auto procedure file.

4.3. Hot to Run the Automatic Test?

1) Copy SAUTO.INF to another name file and Modify 1th option.
2) Use option that is [/f<file_name>] in SSAD command line option

Example)
Copy SAUTO.INF to TEST.INF, modify 1th option.

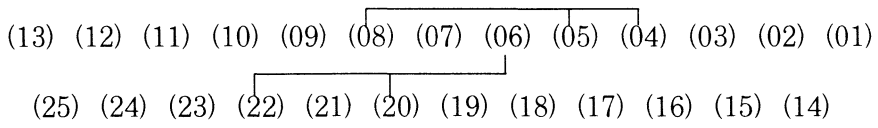
· C\SSAD> SSAD /aw10 /ftest.inf

3) You only can stop the automatic test by using [Ctrl-C] key.

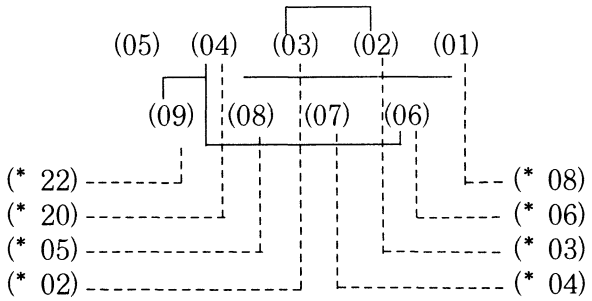
Appendix A. Loopback Connector Diagram

A.1. RS232 Serial Port LoopBack

1) 25 PIN

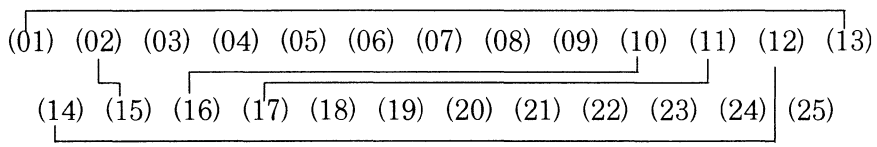


2) 9 PIN



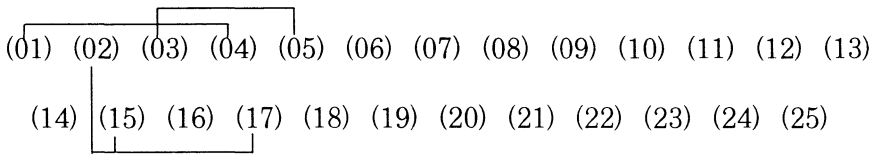
* ... Number of corresponding the 25 PIN

A.2. Parallel Port LoopBack

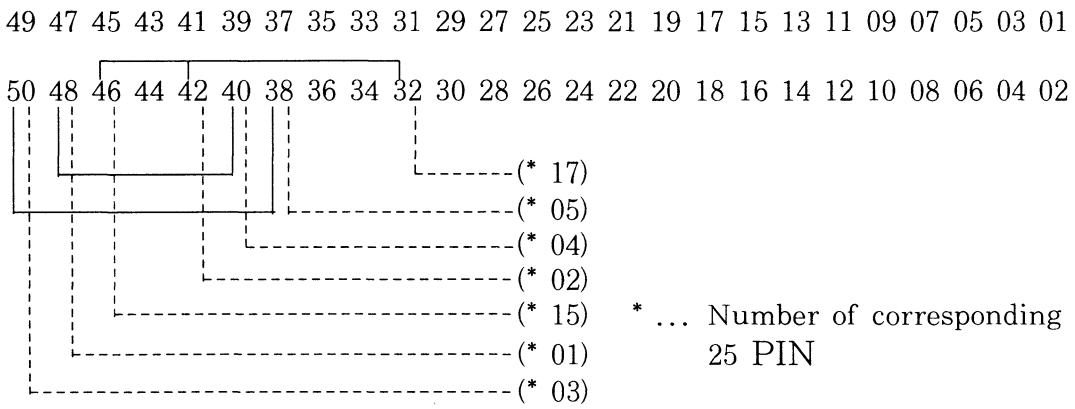


A.3. SCSI LoopBack

1) 25 PIN



2) 50 PIN



* ... Number of corresponding the 25 PIN

Appendix B. Error Message (Include Error Status)

B.1. RAM (System, CMOS) ... [01??]

0100 System RAM 08 xx
- 10H : High Address Bus Short Error
- 20H : Data Bus Short Error
- 30H : Data Pattern R/W Error
- 40H : Even/Odd Bank Access Error
- 50H : Cell Test Data Error
- 51H : Cell Test Address Error

8 0000H - 08 FFFFH (Error block in 64K unit)

0102 CMOS RAM R/W Error 21 04
- 0000 0100 (Error Bit Set)
- Error Address (21H Register)

B.2. ROM (BIOS, Extended BIOS, I/O Card) ... [02??]

0200 BIOS ROM checksum Error
0201 Extended BIOS ROM Error 00AL : byte checksum Error value
- socket on CPU board

0202 I/O Card ROM Error 00AL : byte checksum Error value
- EGA Card BIOS & etc.

B.3. Speaker ... [03??]

0300 Speaker Error

B.4. Mouse ... [04??]

0400 Mouse test Error
04F0 Mouse not installed Error

B.5. NPX (Numeric Processor Extension) ... [05??]

0500	NPX Initialize test Error		
0501	NPX Control Word Initialize test Error	xx xx ——	Control Word
0502	NPX Status Word Initialize test Error	xx xx ——	Status Word
0503	NPX Tag Word Initialize test Error	xx xx ——	Tag Word
0504	NPX 8 Stack Register Xfer test Error		
0505	NPX Status Word test Error		
0506	NPX IE of Status Word test Error	xx xx ——	Status Word
0507	NPX DE of Status Word test Error	xx xx ——	Status Word
0508	NPX ZE of Status Word test Error	xx xx ——	Status Word
0509	NPX UE of Status Word test Error	xx xx ——	Status Word
050A	NPX PE and OE of Status Word test Error	xx xx ——	Status Word
050B	NPX PE of Status Word test Error	xx xx ——	Status Word
050C	NPX Tag Word test Error	xx xx ——	Tag Word

050D	NPX Tag Load, Store test Error	xx xx —— Store Value from NPX
050E	NPX Arithmetic test Error	xx xx —— Status Word
050F	NPX FSAVE, FRSTOR Command test Error	xx xx —— Status Word
0510	NPX 6 EA Exception test Error	
0511	NPX Exception DM test Error	xx xx | └— 13 Status Word low byte └——— 13 NPX Exception occur byte
0512	NPX Exception ZM test Error	Same as above
0513	NPX Exception UM test Error	Same as above
0514	NPX Exception OM test Error	Same as above
0515	NPX Exception IM test Error	Same as above
0516	NPX Exception PM test Error	Same as above

B.6. Keyboard ... [07??]

0700	Keyboard Processor Reset Error	00 0D - received code other than AAH
0701	Keyboard controller BAT Error	
0702	Keyboard Scancode test Error	
07F0	Keyboard layout not exist Error	

B.7. VGA Mode Test ... [08??]

0800	Video display test Error
0801	Color Attribute test Error
0802	Color Character set test Error
0803	80X25 mode test Error
0804	40X25 mode test Error
0805	80X60 mode test Error
0806	100X50 16 color test Error
0807	320X200 palette 0 test Error
0808	320X200 palette 1 test Error
0809	640X200 2 color test Error
080A	640X200 16 color test Error
080B	640X350 16 color test Error
080C	640X480 16 color test Error
080D	720X512 16 color test Error
080E	800X600 16 color test Error
080F	1024X768 16 color test Error
0810	320X200 256 color 1 test Error
0811	320X200 256 color 2 test Error
0812	640X480 256 color test Error
0813	800X600 256 color test Error
0814	1024X768 256 color test Error
0815	1024X768 16 color Non-Interlace mode test Error
0816	1024X768 256 color Non-Interlace mode test Error
0830	8 page change test Error
0831	Text scrolling test Error
0832	2 font display test Error
0833	8 font display test Error
0834	Panning/Split screen test Error

0835 Smooth scroll test Error
08F0 VGA.EXE load & Execute Error

B.8. VGA Chip diagnostics ... 〔09??〕

0900 EGA/VGA Chip test Error
0901 EGA/VGA general Error
0902 Video base RAM test Error
0903 Video RAM 256K test Error
0904 Video RAM 512K test Error
0905 Video RAM 1M test Error
0906 Read mode 0 test Error
0907 Read mode 1 test Error
0908 Write mode 0 test Error
0909 Write mode 1 test Error
090A Write mode 2 test Error
090B Write mode 3 test Error
090C Switch setting test Error
090D Reading inactive plane test Error
090E Reading active plane test Error
090F Rotation function test Error
0910 Linear address test A0-A7 Error
0911 Linear address test A9-A15 Error
0912 Cursor address test A0-A7 Error
0913 Cursor address test A8-A15 Error
0914 Cursor address test A16-A17 Error
0915 Bit mask function test Error
0916 Latched data test Error
0917 Even/Odd mode test Error
0918 CRTC/TS/GDC/ATC test Error
0919 Internal REG test Error
091A Ext palette short test Error
091B Ext palette R/W test Error
091C Translation ROM data test Error

B.9. Floppy Diskette ... 〔0A??〕

0A00 FDD Reset Test Error — d0 00 — d : Error drive (0/1)

0A02 FDD R/W Test Error — xx xx
- h00s ssss — s : Error Sector (1 - 12H)
- h : Error Head (0 / 1)
- dttt tttt — t : Error Track (0 - 4FH)
- d : Error Drive (0 / 1)

0A03 FDD R/W Data Test Error

0A04 FDD Seeking Error — d0 tt — tt : Error Track (0 - 4FH)
- d : Error Drive (0 / 1)

0A05 FDD Motor Speed Error — d1 96 — 196 : Time for one rotation (s)
- d : Error Drive (0 / 1)

0A06 FDD Diskette too many times accessed Error
0AF0 Drive not exist Error

0AF1 Drive not ready Error d0 xx ——— : BIOS(13H) error code(AH)
└———— d : Error Drive (0 / 1)

0AF2 FDD Diskette is unusable Error

B.A. Fixed Disk ... 〔0B??〕

0B00 HDD Reset Error d000 0000 0000 0000 d : Error Drive (0 / 1)

0B02 HDD R/W Test Error dhhh h0tt tttt tttt
| └┘ └──────── t : Error Track (0 - 1023)
| └──────── h : Error Head (0 - 15)
└──────── d : Error Drive (0 / 1)

0B03 HDD Seeking Error d000 00tt tttt tttt — t : Error Track (0 - 1023)
└──────── d : Error Drive (0 / 1)

0B04 HDD ECC Test Error

0B05 HDD Scanning Test Error

0B06 HDD reset in Seeking Test Error

xx xx ——— No meaning
|| || ——— BIOS(13H) error code(AH)

0BF0 Drive not selected Error

B.B. Parallel Port Test ... 〔0C??〕

0C00 PIO Internal Data Port R/W Test Error

0p xx
| └┘ ——— Error Bit Set
└——— Error Port# (LPT 0/1)

0C01 PIO Internal Control Port R/W Test Error

0p xx
| └┘ ——— Error Bit Set
└——— Error Port# (LPT 0/1)

0C02 PIO External Loop-Back Test Error

0p xx
| └┘ ——— 0 0 0 1 1 1 1 1 Error Pin Combination
| | | | | | └— (02) —(15)
└— Error Port# (LPT 0/1) | | | | └——— (01) —(13)
| | | └——— (12) —(14)
| | └——— (10) —(16)
└——— (11) —(17)

0C03 PIO Interrupt Test Error

0p xx
| └┘ ——— No meaning
└——— Error Port# (LPT 0/1)

0C04 Printing test Error

0p xx
| └┘ ——— No meaning
└——— Error Port# (LPT 0/1)

0CF0 Port not selected Error

B.C. Serial Port Test ... [0D??]

0D00 SIO Modem control port test Error xx xx
- xx xx: Test pattern

0D01 SIO Interrupt test Error

0D02 SIO Baudrate test Error 0p xx
- 0p: Error Port# (COM 1/2)
- xx: no meaning

0D03 SIO RxD INT test Error
0D04 SIO TxD INT test Error
0D05 SIO Break INT test Error
0D06 SIO DCD/CTS INT test Error
0D07 SIO DSR/RI INT test Error
0D08 SIO Overrun INT test Error

0p xx
- 0p: Error Port# (COM 1/2)
- xx: no meaning

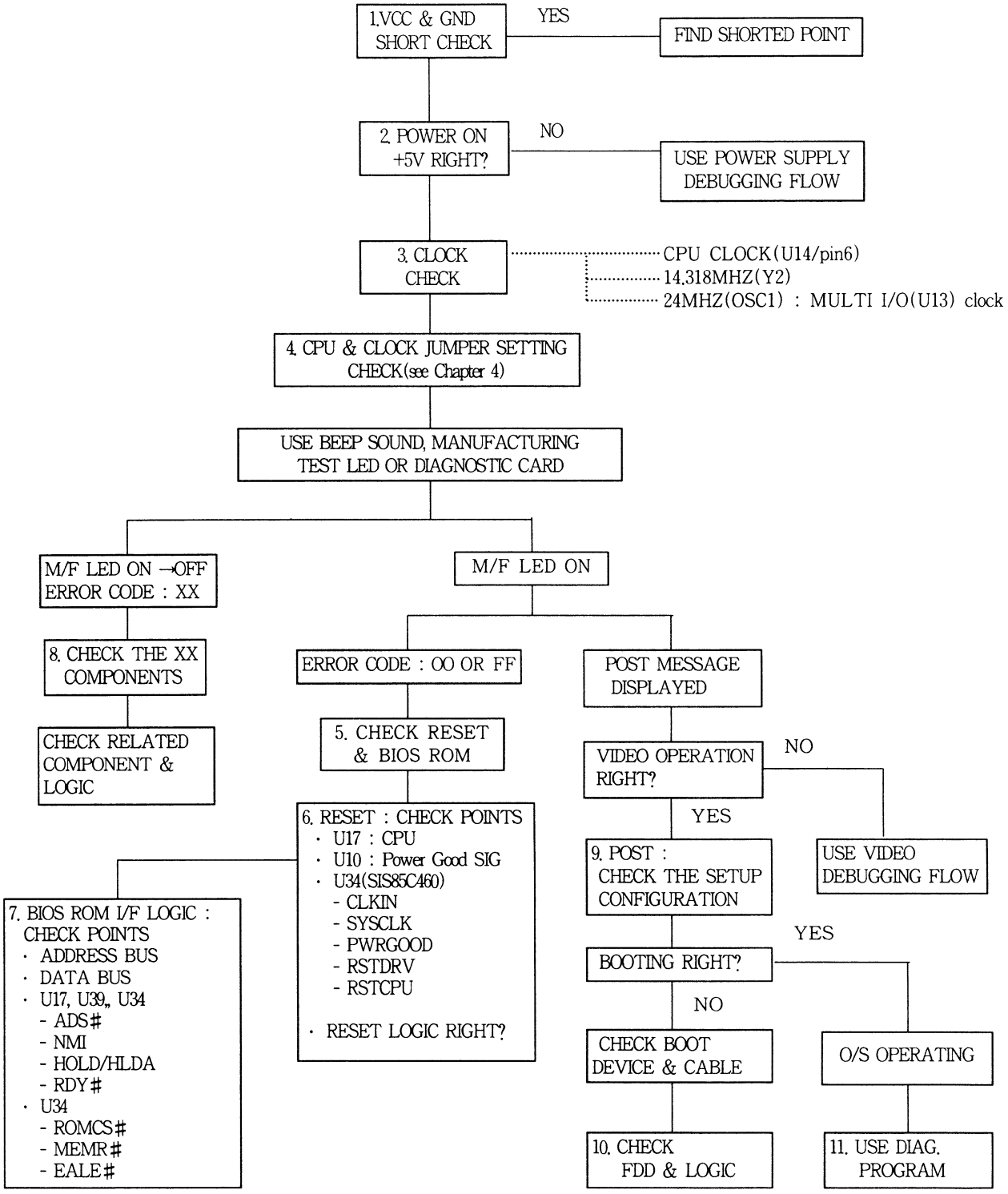
0D09 SIO Data Send/Receive test Error 0p xx
- 0p: Error Port# (COM 1/2)
- xx: Send ASCII

0D0A SIO Loopback status test Error

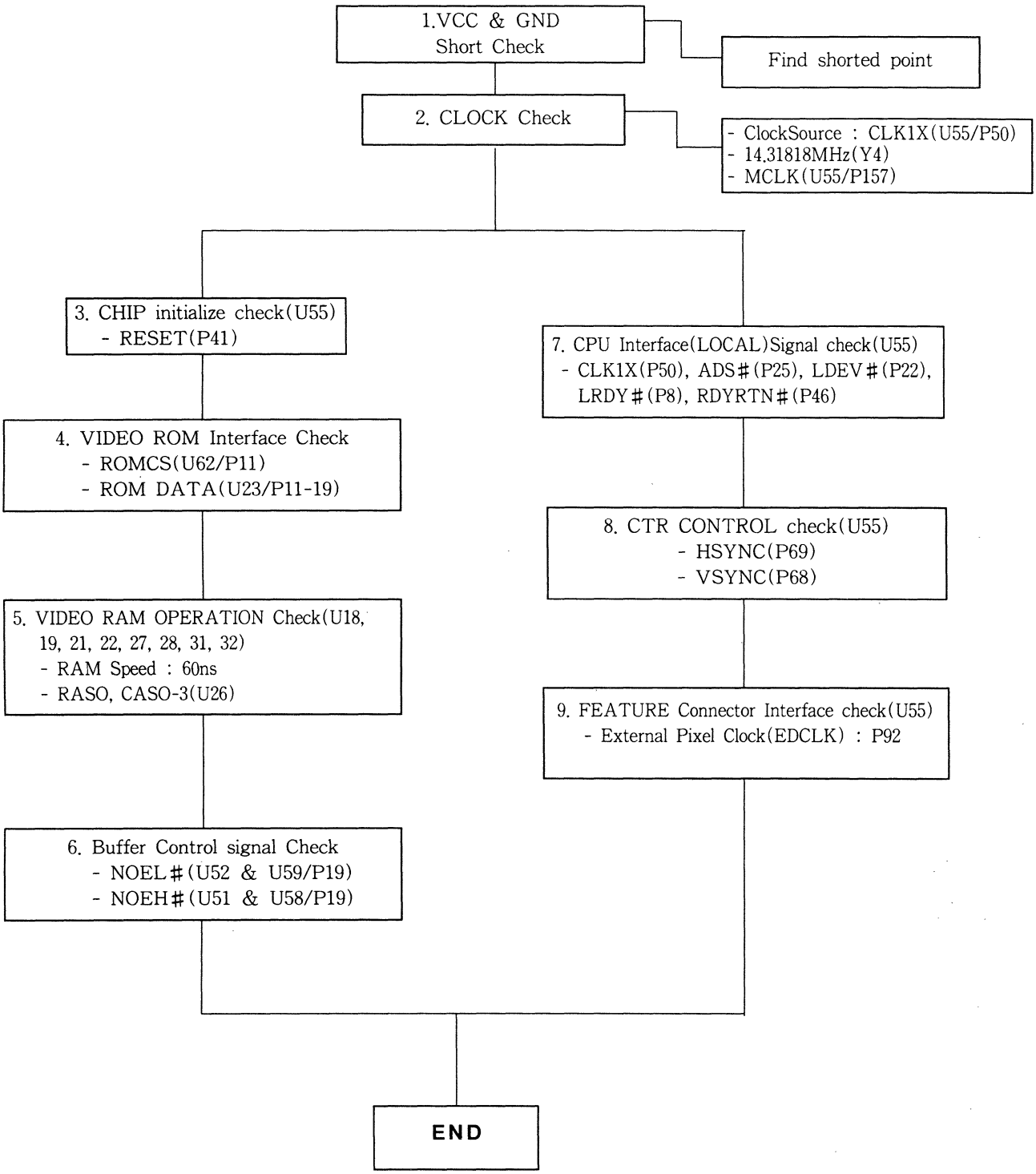
xx xx
- xxxc tfpo
  - o: Overrun Error
  - p: Parity Error
  - f: Framing Error
  - t: Timeout Error
  - c: Error Port (COM 0/1)
- bbb pp s dd
  - pp: x0 None, 01 Odd, 11 Even
  - s: 0 1 stop, 1 2 stop bit
  - dd: 10 7 bit data, 11 8 bit data
  - bbb: 000 110 baud, 001 150 baud, 010 300 baud, 011 600 baud, 100 1200 baud, 101 2400 ″, 110 4800 ″, 111 9600 ″

0D0B SIO Interrupt test timeout Error
0D0C SIO Interrupt baudrate timeout Error
0D0D SIO loopback timeout Error
0DF0 Port not exist Error

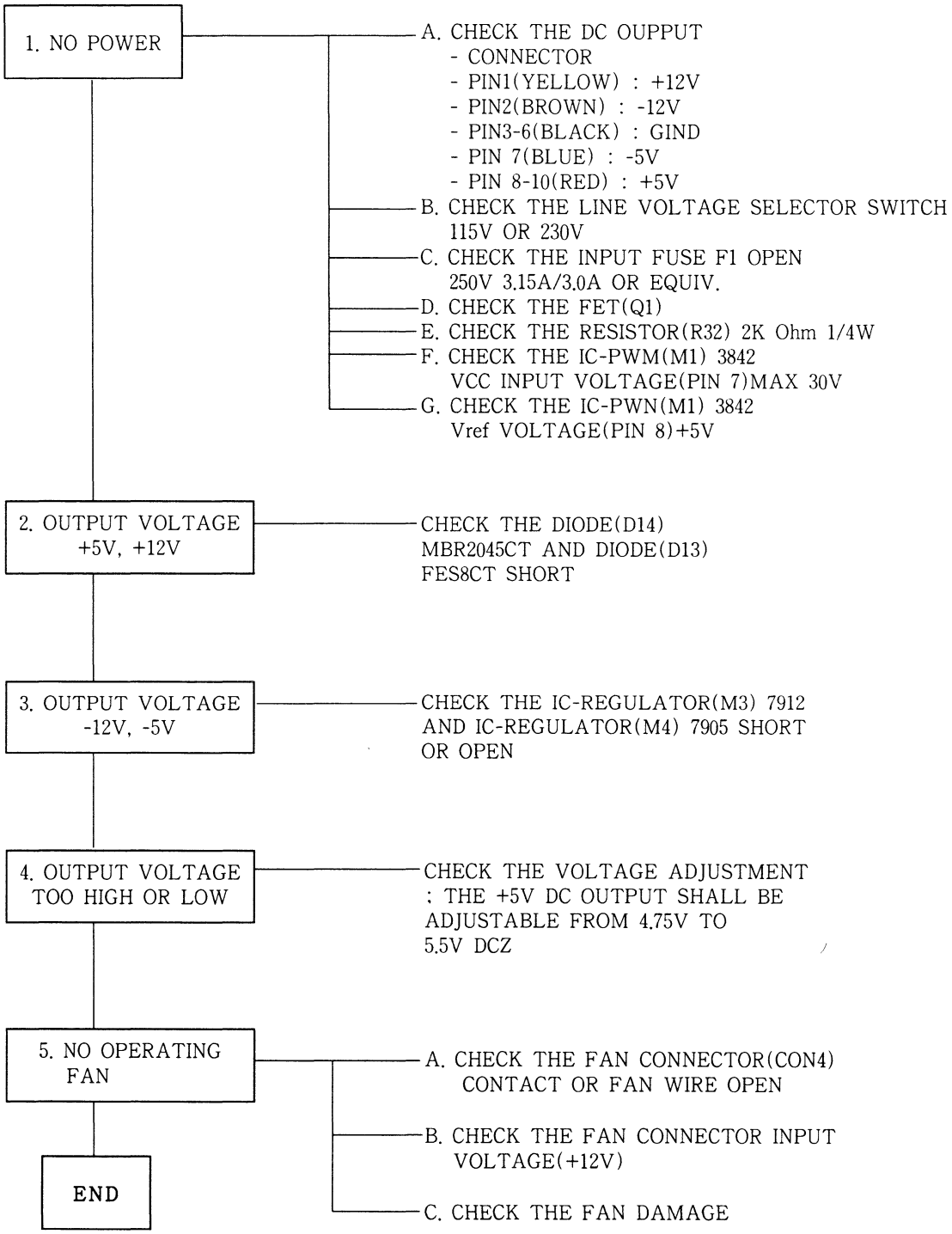
Main Logic Debugging Flow



Video Logic Debugging Flow



Power Supply Debugging Flow



Chapter 3. Chip Set Data Sheet

SiS 85C460 (ISA 386/486 Single Chip)

SiS 85C460 (ISA 386/486 Single Chip)

FEATURES

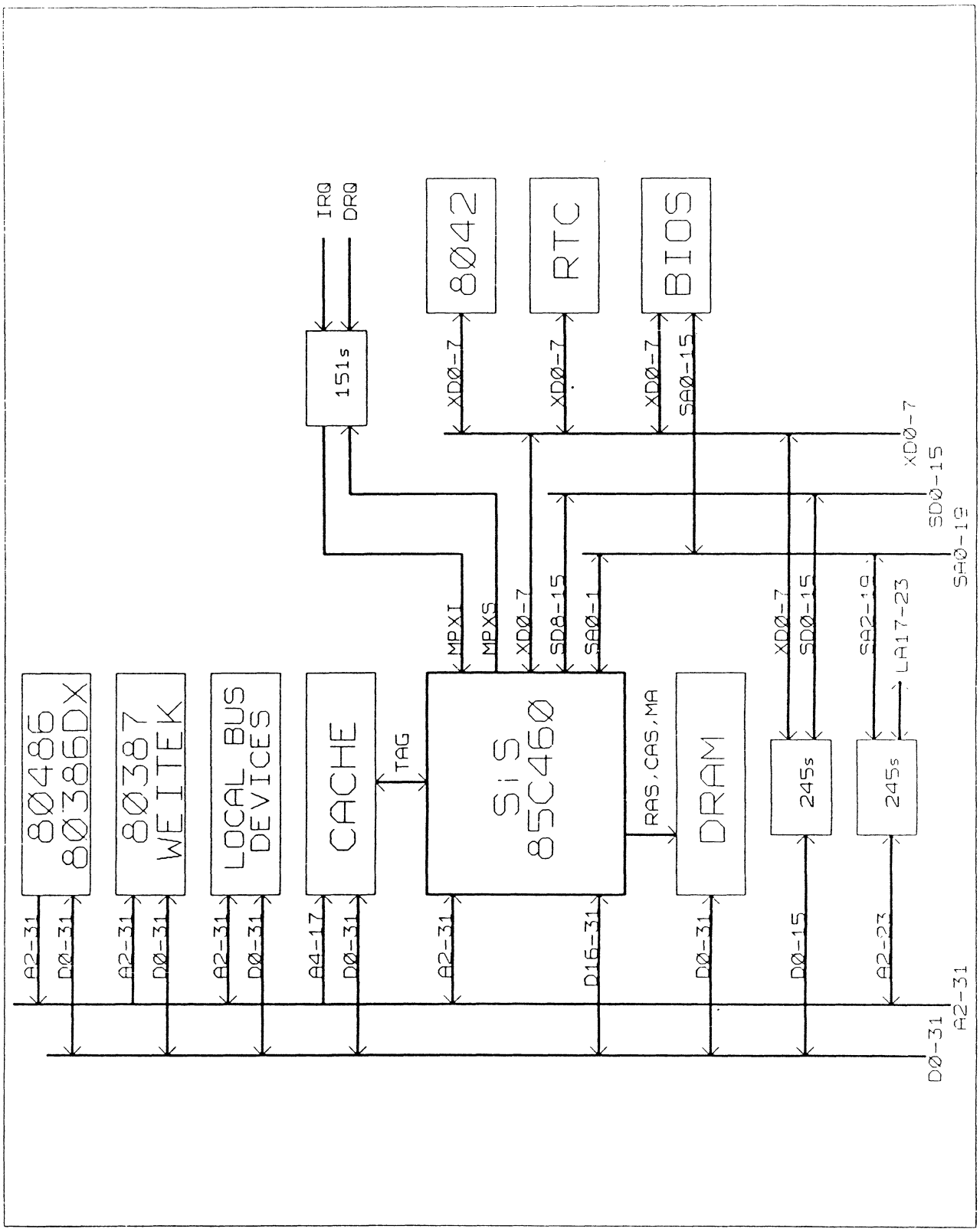
- **Fully IBM PC/AT Compatible 80386DX and 80486DX2/DX/SX Single Chip Controller**
- **Direct Mapped Cache Controller**
  - Write-Back or Write-Through Schemes
  - Bank Interleave/Non-Interleave Cache Access
  - 0/1 Wait State Cache Write Hit
  - Flexible Cache Size: 32/64/128/ 256KB and above
  - Flexible Burst Read Timing Option for 80486 DX/SX Operation: 2-1-1-1, 3-1-1-1, 2-2-2-2 and 3-2-2-2
- **Fast Page Burst Mode DRAM Controller**
  - 4 Banks up to 64MB of DRAM
  - 256K/512K/1M/2M/4MxN DRAM Support
  - Programmable DRAM Speed
- **Two Programmable Non-Cacheable Regions (64KB~4MB)**
- **CAS-before-RAS Transparent DRAM Refresh**
- **BIOS/Video ROM Cacheable**
- **Shadow RAM in Increments of 32KB**
  - Option to Disable Cache in Shadow RAM Area
- **256K Memory Relocation**
- **8042 Emulation of Fast A20GATE and CPU Reset**
- **Hardware/Software De-Turbo Switch**
- **Support 16~40MHz 386DX CPU and 16~50MHz 486 CPU Operation**
- **AT Bus State Machine and AT Bus Controller**
- **Synchronous/Asynchronous AT Bus Clock**
- **Programmable AT Bus Speed**
  - 1/2, 1/3 , 1/4 , 1/5 , 1/6, 1/8, 1/10 of Input Clock or 7.159MHz
- **Programmable Wait State Generation**
  - 1 or 2 Wait States for 16-Bit Transfer
  - 4 or 5 Wait States for 8-Bit Transfer
- **Programmable I/O Recovery Time**
- **32-Bit Data Buffer Between CPU and AT System**
- **Data Conversion and Swapping Logic for 32-/16-/8-Bit Transfer During CPU and DMA Cycles**
- **Data Latch for AT Read Cycle**
- **Parity Generation and Detection Logic**
- **Port B Register and NMI Logic**
- **Integrated Peripheral Controllers**
  - Two 8259A Interrupt Controllers
  - Two 8237 DMA Controllers
  - An 8254 Counter/Timer
  - A 74LS612 Mapper
- **387/487SX and Weitek 3167/4167 Coprocessors Interface**
- **208-Pin PQFP**
- **0.8um Low Power CMOS Technology**

The SiS85C460 is a high performance, 100% PC/AT compatible single chip controller, designed for cache/non-cache 386DX or 486 PC systems running up to 40MHz or 50MHz respectively. The high integration of powerful cache controller, DRAM controller, CPU interface, bus controller, data buffers and peripheral controllers provide an easy and very economical solution for compact board manufacturing.

The SiS85C460 contains a built-in cache controller which provides direct mapped write-through/ write-back schemes. The programmable AT-bus clock supports compatible AT-bus timing for different PC system. Besides, the local bus interface and the integration of DMA Controller, Interrupt Controller and Timer/Counter are designed to give a high performance, compact, and cost-effective product for a 386DX or 486DX/SX PC/AT system.

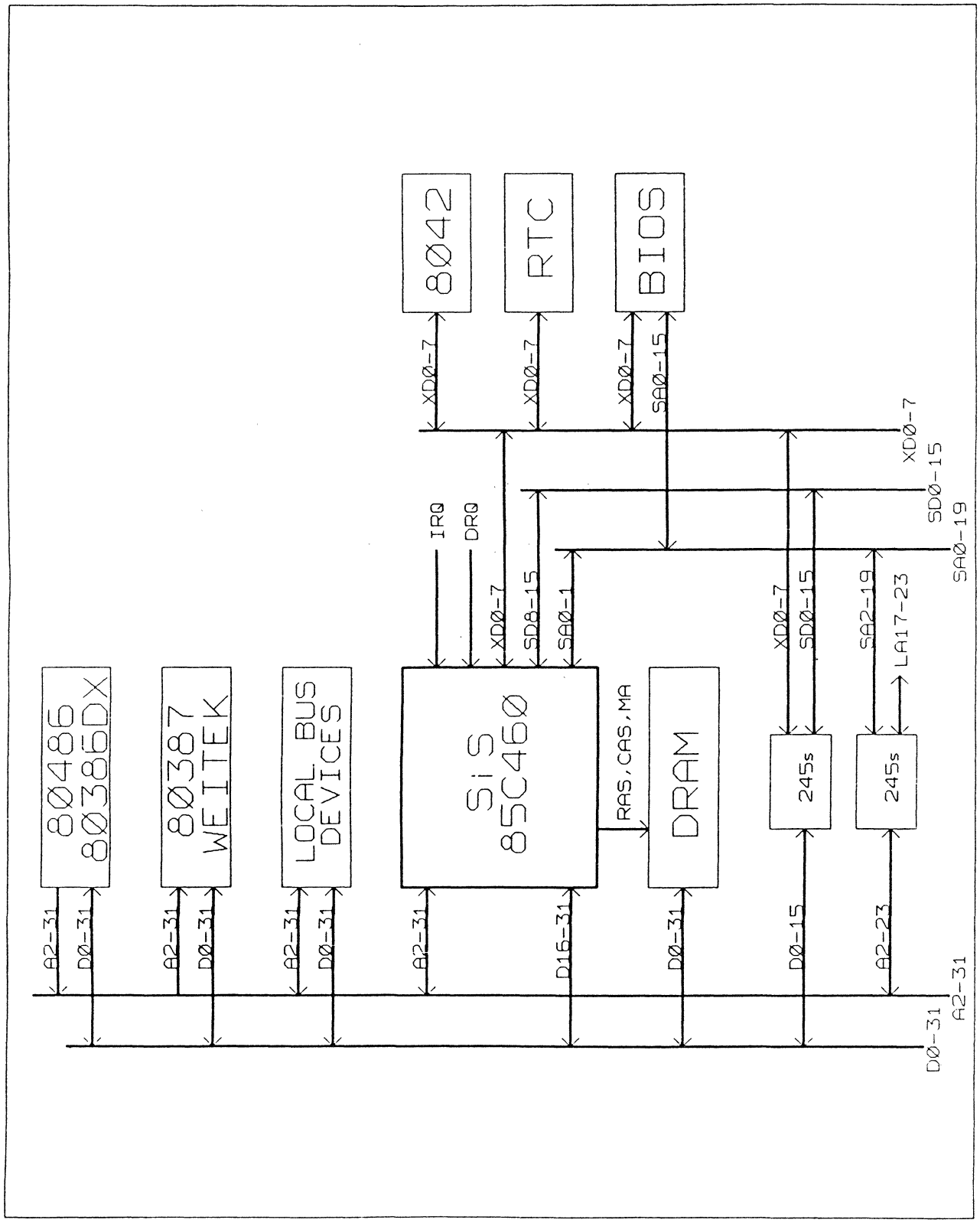
FUNCTIONAL BLOCK DIAGRAM

With CACHE application



FUNCTIONAL BLOCK DIAGRAM (continued)

Without CACHE application



FUNCTIONAL DESCRIPTION

Cache Controller

Direct Mapped Cache

Cache is a good means to de-couple fast processor from slow main memory and get the best performance of the processor. Direct mapped cache is the most straightforward, flexible, easy-to-implement, and cost-effective cache structure. A 2/4-way set associative cache has better performance than the direct mapped cache, but the delta is negligible when the cache size is large enough (e.g. 64KB). The SiS85C460 provides a fast 8-bit tag comparator and all the control logic for a cache of the 80486 processor. To implement a cache, user just needs to add SRAMs for the tag and data memories. The maximum cache size in the configuration register is 256KB but larger (512KB, 1MB, etc.) size is still applicable.

Write-Back vs. Write-Through

When the contents of the cache data are modified (i.e. written) by the processor, the same changes should be made in the main memory as well. Failing to do so will raise an inconsistency problem when the stale data in the main memory are accessed. There are two general approaches to update the main memory. The first is the write-through method and the second is the write-back (also called "copy-back") method.

In a write-through cache system, data are written to the main memory immediately while or after they are written into the cache. So the main memory always contains valid data. All the memory writes will only be as fast as the DRAM write and do not take the speed advantage of the cache.

In a write-back cache system, there is an "alter" bit per data LINE (data line means the data block referenced to a specific tag). When a write hit happens on the cache, the corresponding alter bit will be set. The written data are transferred to the main memory when they are to be over-written by a cache line fill. In this case, the cache controller checks the corresponding alter bit. If the alter bit is set, the cache data will then be written to the main memory before the cache line fill starts.

A write-back cache can offer higher performance than a write-through cache if writes to the main memory are much slower than writes to the cache. The write-back cache is also favored when a memory location is written several times in the cache before written into the main memory. The performance advantage of the write-back cache over write-through cache is software dependent.

The SiS85C460 can be configured to provide a write-back or write-through cache scheme. Besides tag and data RAM, a write-back cache needs an SRAM for the alter bits. So a write-back cache may have better performance, but costs more, than a write-through cache does. It is up to the indivisual user to judge if the extra cost of the write-back cache is justified.

80486 Burst Cache Line Fill

The internal cache of the 80486 has a 16-byte line size. When a read miss happens in the internal cache, the 80486 initiates off-chip memory read cycles to update current cache line. The 80486 will read 16 continuous bytes (4 doublewords). To increase the bus throughput, the 80486 provides a burst mode transfer, four doublewords can be read sequentially in 5 processor clocks (2-1-1-1) at the fastest.

The external cache provided by the SiS85C460 also has a 16-byte line size. It supports the 80486 burst read cycles to get the fastest cache line fill. When both the 80486 internal and external caches encounter a read miss, they are updated with the data read from DRAM simultaneously.

Cache Update Policy

For CPU cycles, the content of the cache memory is renewed when either the cache read miss or write hit occurs. Tag and data RAMs are both updated in the cache read miss cycles. In the cache write hit cycles, the SiS85C460 updates only the data RAM. In the cache write miss cycles, the CPU writes data into the main memory (DRAM), while the cache memory remains unchanged. The alter bits in the write-back cache are reset in the cache update (read miss) cycles and set in the write hit cycles.

When the cache is disabled, all the CPU reads to the cacheable memory are treated as cache read miss, so both tag and data RAMs are updated. This feature is used to initialize the cache memory before enabling it.

In DMA/master cycles, the cache data RAM is written when a write hit occurs, to assure the cache coherency. Cache memory is not accessed in DMA/master write miss or read cycles for the write-through cache. For the write-back cache, DMA/master read hit cycles are conducted to the cache, not to the DRAM.

Cache Size Options

Cache Size	Tag RAM	Data RAM	Alter RAM	Cacheable Size
32KB	2Kx8	8Kx8 x4	2Kx1	8MB
64KB	4Kx8	8Kx8 x8	4Kx1	16MB
128KB	8Kx8	32Kx8 x4	8Kx1	32MB
256KB	16Kx8	32Kx8 x8	16Kx1	64MB
512KB	32Kx8	128Kx8 x4	32Kx1	64MB

The cacheable DRAM size is determined by the cache size because the tag address field is always 8-bit wide. The on-board DRAM beyond the cacheable size is not cacheable. It is still cacheable for the 80486 internal cache, however.

Cache Speed Options for 386 Mode

The SiS85C360 provides two cache read speed options : 2T or 3T, and two options of cache write cycle : 2T or 3T. The 2T cache write is applicable only when the cache read is also set to 2T.

The following is a table of cache configurations and suggested speed ratings of the SRAM for implementing the cache data RAM for various speeds of the 80386 CPU.

Read Cycle-Write Cycle	25MHz CPU	33MHz CPU	40MHz CPU
2T-2T	-35	-20	-12
2T-3T	-40	-25	-20
3T-3T	-65	-45	-35

The following is a table of cache configurations and suggested speed ratings of the SRAM for implementing the cache tag and alter RAM for various speeds of the 80386 CPU.

Read Cycle-Write Cycle	25MHz CPU	33MHz CPU	40MHz CPU
2T-2T	-25	-20	-12
2T-3T	-35	-25	-15
3T-3T	-45	-35	-25

Cache Speed Options for 486 Mode

The external cache can be configurated to non-interleave or two-bank interleave. Two-bank interleaved cache can use slower cache data RAM but needs more data RAM chips.

The SiS85C460 provides four cache read speed options : 2-1-1-1, 3-1-1-1, 2-2-2-2 and 3-2-2-2, and two options of cache write cycle : 2T or 3T. The cache read speed x-y-y-y is selected via the bit 7 of configuration register 50 (x) and the bit 0 of configuration register 51 (y). The 2T cache write is applicable only when the first cache read of a burst is also set to 2T (2-1-1-1 or 2-2-2-2).

The following is a table of cache configurations and suggested speed ratings of the SRAM for implementing the cache data RAM for various speeds of the 80486 CPU.

Cache Configuration	25MHz CPU	33MHz CPU	40MHz CPU	50MHz CPU
2-1-2 Interleave (*1)	-35 (*2)	-20	-12	----
2-1-2 Non-interleave	-25	-15	----	----
2-1-3 Interleave	-40	-25	-20	----
2-1-3 Non-interleave	-25	-15	----	----
3-1-3 Interleave	-45	-25	-20	-12
3-1-3 Non-interleave	-25	-15	----	----
2-2-2 Non-interleave	-35	-20	-12	----
2-2-3 Non-interleave	-40	-25	-20	----
3-2-3 Non-interleave	-65	-45	-35	-25
3-2-3 Interleave	-80	-55	-45	-30

Note: *1. x-y-z means x-y-y-y burst read and zT write cycle.
***2. -m means the access speed of SRAM in ns.**

The following is a table of cache configurations and suggested speed ratings of the SRAM for implementing the cache tag and alter RAM for various speeds of the 80486 CPU.

Cache Configuration	25MHz CPU	33MHz CPU	40MHz CPU	50MHz CPU
2-X-2	-25	-20	-12	----
2-X-3	-35	-25	-15	----
3-X-3	-45	-35	-25	-20

Note: X presents either 1T or 2T cycles.

Non-Cacheable Regions

In some applications, users desire a block of memory not to be cached. The SiS85C460 provides two programmable non-cacheable regions to serve this function.

Only the on-board DRAM directly controlled by the SiS85C460 is cacheable. The memory residing on the AT add-ons is non-cacheable. When a memory space is mapped by both the on-board DRAM and AT add-on memory, CPU access will be conducted to the on-board DRAM. If users desire the AT add-on memory to be accessed instead of the on-board DRAM at the overlapped memory space, the two non-cacheable regions can be used to disable the on-board DRAM in the programmed space.

The size and starting address of two non-cacheable regions are programmable in configuration register 54, 55, 56 and 57. The validity of the starting address bits depends on the size of related non-cacheable region.

Size	A23	A22	A21	A20	A19	A18	A17	A16
64K	V	V	V	V	V	V	V	V
128K	V	V	V	V	V	V	V	X
256K	V	V	V	V	V	V	X	X
512K	V	V	V	V	V	X	X	X
1M	V	V	V	V	X	X	X	X
2M	V	V	V	X	X	X	X	X
4M	V	V	X	X	X	X	X	X

V = Valid
X = Don't Care

Cache Initialization

The external cache supported by the SiS85C460 does NOT provide the validation flag (bit) for the data lines. All the cache data are assumed valid once the cache is enabled. So the whole cache must be filled by valid data before the cache enable bit is turned on. The cache initialization can be done via sequential reads to a block of on-board DRAM which is equal to or larger than the cache in size.

DRAM Controller

DRAM Speed Options

The SiS85C460 provides 4 read and 2 write speed options in the configuration register. A table of page hit cycle time of all the possible speed configurations is listed as follows:

	Read	486 Burst Read	Write
Fastest	3	3-2-2-2	2
Faster	4	4-3-3-3	2/3
Slower	5	5-4-4-4	2/3
Slowest	6	6-5-5-5	4

Note: The unit of the above table is in T cycles.

There will be plenty of timing margin if the user adopt, Fastest for 25MHz 80386/80486, Faster for 33MHz, Slower for 40MHz, and Slowest only for 50MHz 80486.

DRAM Access Timing

	Fastest	Faster	Slower	Slowest	
Trcd	1.5T	2T	2T	3T	RAS-to-CAS delay
Tcas	1.5T	2T	3T	3T	Read CAS pulse width
Trp	3T	3T	4T	4T	RAS precharge
Tcp	0.5T	1T	1T	2T	CAS precharge

DRAM Size Configuration

The SiS85C460 supports 32 different DRAM configurations in 4 banks. Besides the traditional 256K/1M/4M xN DRAMs, the new 512K xN and future 2M xN DRAMs are also supported.

Refresh

In the original PC/AT design, the CPU is held off (i.e. can not do anything) during the DRAM refresh cycles. It happens once per 15us and takes at least 0.5us each time. In SiS85C460, refresh can be selected to hold CPU or not by setting the bit 5 of the configuration register 58.

Recently the speed of DRAM is becoming faster so the time needed per refresh cycle is getting shorter. The refresh cycle time for the 100ns DRAM is 200ns minimum, for example. In a system with cache, most of the CPU accesses are referred to the cache so that the DRAM usage (percent of time the DRAM is accessed by the CPU) is significantly reduced.

In the SiS85C460, the main memory refresh is independent to the AT-bus refresh so the cycle time is shorter (need not follow the standard AT-bus timing). When the main memory is refreshed, the CPU is NOT held off so it may execute the program stored in the cache at the same time. If the CPU accesses the main memory while it is being refreshed, this access will be pending (i.e. the CPU must wait) until the refresh is finished.

The following table lists the refresh-related RAS timings of the on-board DRAM:

	Fastest	Faster	Slower	Slowest
RAS pre-charge	3T	3T	4T	5T
RAS active	3T	4T	4T	5T

If hidden refresh is selected on AT bus, the AT bus refresh cycles are issued once per 15us when there is no access from the CPU, the DMA controller, or the bus master on the AT bus. The CPU will not feel the existing of the AT bus refresh unless it issues an AT cycle or cache miss cycle coincidentaly. The controller arbitrates among the CPU AT cycle, DMA/master request, and bus refresh so that they can be executed one after another when more than one of them intend to use the AT bus at the same time.

The SiS85C460 has a slow refresh feature to cut the refresh frequency down to 1/4. It should be selected only when the system is equipped with slow-refresh DRAM.

The refresh scheme of local DRAM is the CAS-before-RAS refresh. The CASs go active at least one T before RASs in local refresh. To reduce the power noise caused by refresh, the RASs of odd banks go active one T after that of even banks. It is called "staggered refresh".

Shadow RAM

Memory space 0A0000-0FFFFFh is reserved for the video RAM, I/O and system BIOS ROM. Access to this area should not be conducted to the main memory in standard PC/AT. Since the speed of the DRAM is significantly faster than that of the ROM, if contents of the BIOS ROM are copied to the unused DRAM (0A0000- 0FFFFFh), the DRAM can work as fast BIOS ROM and raise the overall system performance. This is called the "Shadow RAM".

The SiS85C460 provides shadow to 0C0000-0EFFFFh in 32KB granularity and shadow to 0F0000-0FFFFFh. The shadow RAM is default non-cacheable. The shadow RAM in C0000-C7FFFh, and F0000-FFFFFh can be programmed to be cacheable.

256KB Relocation

The SiS85C460 provides the 256KB DRAM relocation from 0A0000-0BFFFFh and 0D0000-0EFFFFh to the top of configurated DRAM size.

This function works for the DRAM sizes of 1MB, 2MB, 4MB, 6MB and 8MB when the shadowing of segments D and E is disabled.

ROM Support

The SiS85C460 provides a chip select signal for the system BIOS ROM. The memory space assigned to the ROM is the highest 64/128KB of the real (1MB) and the protected (4GB) address modes of the 80486/80386DX CPUs.

The system BIOS ROM can be shadowed by the DRAM to improve performance. When the shadow RAM is turned on, the access to system BIOS with address below 100000h will be channeled to the DRAM.

Fast A20GATE And CPU Reset

In the original PC/AT design, the A20GATE and CPU Reset (RC) are controlled by the 8042 keyboard controller to switch the CPU between the real and protected address modes. The operation of 8042 is quite slow so if the address mode switching happens frequently, the program execution speed will be affected.

The SiS85C460 provides a 8042 emulation to generate the A20GATE and CPU reset in hardware. This feature is software transparent.

Local Bus Support

The SiS85C460 uses LBD* (stands for Local Bus Device) and LRDY* (stands for Local Bus Device Ready) pins to implement "Local Bus Device Architecture" such as Weitek 3167/4167. The interface protocol is very straightforward.

When a local bus device decodes the bus definition/address from CPU and finds the cycle belonging to it at the start of a CPU bus cycle, it should assert LBD* to inform the SiS85C460 that it's a local bus device cycle. The SiS85C460 will operate a local bus cycle, until either LRDY* is asserted from the local bus device to SiS85C460 to generate CPURDY*, or the local bus device asserts CPURDY* (wire-OR with the CPURDY* of SiS85C460) itself to terminate current cycle. In the former case, the SiS85C460 will synchronize LRDY* with CCLKIN then asserts CPURDY*. In the later case, the SiS85C460 detects the asserted CPURDY* to finish the current cycle.

When there is more than one local bus devices, their LBD* and LRDY* signals should be ANDed together before connecting to the SiS85C460.

The SiS85C460 samples the LBD* input at the end of T2 when DRAM speed is set to "FASTEST" or "FASTER", and at the end of T3 when DRAM speed is "SLOWER" or "SLOWEST". The LBD* pin should be asserted before the sampling point, when the current cycle is a local bus cycle.

The implementation to support full VESA VL-Bus specification will be provided in the future version of silicon.

Turbo Switch

Some old applications may get into trouble if the system speed is too fast. The SiS85C460 offer a de-turbo function that can be controlled through a hardware switch or software programming. When the de-turbo function is turned on, system performs 1/3 or 2/3 speed selected by the bit 4 of configuration register 58.

Clock Generation

The SiS85C460 provides a flexible software controlled selection of the clock used for the AT bus state machine. Bus clock is determined by the configuration register and can be selected as 1/2, 1/3, 1/4, 1/5, 1/6, 1/8, 1/10 of the input clock or 7.159 MHz.

The clock switches speed automatically, with clean transition, whenever the configuration is changed.

AT Bus State Machine

In order to obtain the maximum performance of the system board, it is desired to run the system board at the maximum CPU frequency. This frequency may be too fast for the slow AT bus. In order to overcome this problem, the SiS85C460 operates the state machine at a slower frequency than the CPU frequency.

The SiS85C460 starts a bus cycle when an BS16* is active and an BALE signal has been inserted in the AT-TS state. It then enters the command cycle AT-TC and provides the timing signals for AT bus cycle and terminates by asserting READY* signal. To determine the bus size, MEMCS16* signal is sampled at the falling edge of BALE during memory cycle. IOCS16* is sampled at every rising edge of SYSCLK after the command is active in an I/O cycle.

The command cycle is terminated only when IORDY* is active and all programmed wait states have been executed. The period of command cycle is selected by the configuration register. For 16-bit transfer, the default is 1 wait state, but can be selected as 2 wait states. For 8-bit transfer, the default is 5 wait states, but can be selected as 4 wait states. No command delay is inserted for 16-bit memory cycle, otherwise 1/2 SYSCLK command delay is always inserted.

IORDY* is sampled at the start of every AT-TC state. The command cycle will not be terminated until IORDY* is sampled HIGH and all programmed wait states have been executed. If ZWS* is detected LOW at the middle of the AT-TC state, the current AT cycle will be terminated immediately.

During read cycle, the data read from device may be lost after the command is finished. The SiS85C460 will latch the data immediately after the read command is inactive and will hold the data until the AT cycle is ended. The "Read Latch" function is active for all AT bus read cycle, except during DMA, Master, or local RAM read cycle.

The shortest command recovery time is two SYSCLK in this chip, this could be too short for some I/O devices. In this case, a configuration register option is provided. If selected, the I/O command recovery time will be at least 2 SYSCLK for 16-bit transfer and 4 SYSCLK for 8-bit transfer.

Data Conversion Logic

If MEMCS16* and IOCS16* signals are sampled HIGH, the current cycle will be an 8-bit transfer cycle. The AT state machine performs data conversion if the CPU executes a 16-bit read or write during an 8-bit transfer. The SiS85C460 separates a 16-bit read or write operation into two 8-bit transfers and activates SA0 signal in the second cycle. Meanwhile, the SiS85C460 will execute all the data swapping process between the 32-bit, 16-bit and 8-bit data bus.

Besides data conversion cycle, the data will also be swapped if it is necessary during AT cycle. In DMA and Master cycles, the data swapping is also needed. The system checks the command, address, and related control signals and then arranges required swapping.

Since the BE0*-BE3* can not be used to select the devices on AT bus directly, BE0*-BE3* will be inputed in AT cycle to generate the SA1, SA0, and BHE* signals needed. In DMA cycle, BE0*-BE3* is generated from the SA1 and SA0 to access the local memory. The SiS85C460 checks these four byte enable signals in AT cycle and determines whether it is a 16-bit read or write and whether data conversion cycle should be performed.

Port B Register and NMI Logic

The SiS85C460 provides access to Port B as defined for IBM PC/AT, as shown below:

Bit	Contents
0	GATE2 - Timer 2 Gate
1	SPKEN - Speaker Data
2	PCKEN - Parity Check Enable
3	IOCHCKEN - I/O Channel Check Enable
4	REFRESH - Refresh Detect
5	OUT2 - Timer 2 Out
6	IOCHCK - I/O Channel Check
7	PCK - Parity Check

The NMI logic in the SiS85C460 will enable and latch the I/O and parity errors to generate a non-maskable interrupt to the CPU, if NMI has been enabled. NMI is enabled when data bit 7 of port 70h is set to 0, and NMI is disabled if it is equal to 1.

Bus Buffer Control Logic

During AT-bus read cycle, the data from device will be latched immediately after the read command is inactive and will be hold till the end of AT cycle.

The SiS85C460 provides 16-bit to 8-bit or 8-bit to 16-bit data bus conversion in AT cycle, and 32-, 16- and 8-bit data bus conversion in DMA cycle.

Parity Generation and Detection

During DRAM write cycles, the SiS85C460 generates even parity for each of the four bytes. The parity bits PD0-PD3 are written to the parity memory in the system DRAM. During the system DRAM read cycles, the SiS85C460 checks for even parity for each byte read. If odd parity is detected, the SiS85C460 flags a parity error. The SiS85C460 detects the error and generates the NMI when enabled. The parity error can be cleared by programming parity check disable, which is defined by bit-2 of the port B register.

Peripheral Controllers

The SiS85C460 contains Peripheral Controllers which include two 8237 DMA Controllers, a 74LS612 Mapper, two 8259 Interrupt Controllers, and an 8254 Counter/Timer.

DMA Controllers

Two DMA controllers are connected in such a way as to provide the user with four DMA channels (DMA1) for 8-bit transfers and three DMA channels (DMA2) for 16-bit transfers (the first 16-bit DMA channel is used for cascading). Included as part of the DMA subsystem is the Page Register (DMA PAGE) device which is used to supplement the DMA and drive the upper address lines when required.

Interrupt Controllers

Sixteen interrupt channels are provided in the SiS85C460. These channels are allocated to two cascaded controllers (INTC1, INTC2) with 8 inputs each. Of these 16 channels, two are connected internally to various devices, allowing 14 user definable interrupt channels. The two internally connected channels are as follows:
Channel 0 - Counter/Timer Counter 0 Interrupt
Channel 2 - Cascade to Slave Interrupt Controller (INTC2)

Counter/Timer

A Counter/Timer (CTC) subsystem contains three independent counters. The clock input for each counter is connected to a clock of 1.19MHz, which is derived by dividing the 14.318MHz crystal input by 12. Counter 0 is connected to Interrupt 0 of INTC1. It is intended to be used as a multi-level interrupt to the system for such tasks as time keeping and task-switching. Counter 1 may be programmed to generate pulses or square waves for used by external devices. The third channel (Counter 2) is a full function Counter/Timer which has a gate input for controlling the internal counter. This channel can be used as an interval counter, a timer, or as a gated rate/pulse generator.

Clock and Wait State Control

The Clock and Wait State Control subsystem performs four functions, control of the DMA command width, control of the CPU read or write cycle length, and selection of the DMA clock rate. All of these functions are user selectable by writing to the Configuration Register located at address 023h.

Writing and reading this register is accomplished by first writing a 01h to locaton 022h to select the Configuration Register, and then performing either a read or write to location 023h.

Peripheral Controllers Address Map

DMA Controller Address Map

DMA1	DMA2	XIOR#	XIOW#	FliP Flop	Register Function
000h	0C0h	0	1	0	Read channel 0 current address low byte
		0	1	1	Read channel 0 current address high byte
		1	0	0	Write channel 0 base and current address low byte
		1	0	1	Write channel 0 base and current address high byte
001h	0C2h	0	1	0	Read channel 0 current word count low byte
		0	1	1	Read channel 0 current word count high byte
		1	0	0	Write channel 0 base and current word count low byte
		1	0	1	Write channel 0 base and current word count high byte
002h	0C4h	0	1	0	Read channel 1 current address low byte
		0	1	1	Read channel 1 current address high byte
		1	0	0	Write channel 1 base and current address low byte
		1	0	1	Write channel 1 base and current address high byte
003h	0C6h	0	1	0	Read channel 1 current word count low byte
		0	1	1	Read channel 1 current word count high byte
		1	0	0	Write channel 1 base and current word count low byte
		1	0	1	Write channel 1 base and current word count high byte
004h	0C8h	0	1	0	Read channel 2 current address low byte
		0	1	1	Read channel 2 current address high byte
		1	0	0	Write channel 2 base and current address low byte
		1	0	1	Write channel 2 base and current address high byte
005h	0CAh	0	1	0	Read channel 2 current word count low byte
		0	1	1	Read channel 2 current word count high byte
		1	0	0	Write channel 2 base and current word count low byte
		1	0	1	Write channel 2 base and current word count high byte
006h	0CCh	0	1	0	Read channel 3 current address low byte
		0	1	1	Read channel 3 current address high byte
		1	0	0	Write channel 3 base and current address low byte
		1	0	1	Write channel 3 base and current address high byte
007h	0CEh	0	1	0	Read channel 3 current word count low byte
		0	1	1	Read channel 3 current word count high byte
		1	0	0	Write channel 3 base and current word count low byte
		1	0	1	Write channel 3 base and current word count high byte

An internal flip-flop is used to supplement the addressing of the Count and Address registers. This bit selects between high and low bytes of these registers and toggles each time a read or write occurs to any of these registers.

DMA Controller Address Map (continued)

DMA1	DMA2	XIOR#	XIOW#	Flip Flop	Register Function
008h	0D0h	0	1	X	Read status register
		1	0	X	Write command register
009h	0D2h	0	1	X	Read DMA request register
		1	0	X	Write DMA request register
00Ah	0D4h	0	1	X	Read mode register
		1	0	Z	Write single bit DMA request mask register
00Bh	0D6h	0	1	X	Read mode register
		1	0	X	Write mode register
00Ch	0D8h	0	1	X	Set byte pointer flip-flop
		1	0	X	Clear byte pointer flip-flop
00Dh	0DAh	0	1	X	Read temporary register Master clear
00Eh	0DCh	0	1	X	Clear mode register counter
		1	0	X	Clear all DMA request mask register bits
00Fh	0DEh	0	1	X	Read all DMA request mask register bits
		1	0	X	Write all DMA request mask register bits

DMA Address Extension Register Map

Address	Register Function
080h	Unused
081h	8-bit DMA Channel 2 (DACK2)
082h	8-bit DMA Channel 3 (DACK3)
083h	8-bit DMA Channel 1 (DACK1)
084h	Unused
085h	Unused
086h	Unused
087h	8-bit DMA Channel 0 (DACK0)
088h	Unused
089h	16-bit DMA Channel 2 (DACK6)
08Ah	16-bit DMA Channel 3 (DACK7)
08Bh	16-bit DMA Channel 1 (DACK5)
08Ch	Unused
08Dh	Unused
08Eh	Unused
08Fh	Refresh cycle

Interrupt Controller Address Map

Register	Type	I/O Port	b7	b6	b5	b4	b3	b2	b1	b0
ICW1	WRO	20h (A0h)	X	X	X	SI	LTM	X	SM	X
ICW2	WRO	21h (A1h)	V7	V6	V5	V4	V3	X	X	X
ICW3	WRO	21h	S7	S6	S5	S4	S3	S2	S1	S0
ICW3	WRO	A1h	0	0	0	0	0	ID2	ID1	ID0
ICW4	WRO	21h (A1h)	X	X	X	EMI	X	X	AEOI	X
OCW1	RD/WR	21h (A1h)	M7	M6	M5	M4	M3	M2	M1	M0
OCW2	WRO	20h (A0h)	R	SL	EOI	SI	2/3	L2	L1	L0
OCW3	WRO	20h (A0h)	0	ESSM	SMM	SI	2/3	PM	RR	RIS
IR	RDO	20h (A0h)	IR7	IR6	IR5	IR4	IR3	IR2	IR1	IR0
IS	RDO	20h (A0h)	IS7	IS6	IS5	IS4	IS3	IS2	IS1	IS0

Note:

WRO = Write only register
RDO = Read only register
RD/WR = Read/Write register
X = Don't care

Counter/Timer Address Map

Address	Function
040h	Counter 0 read/write
041h	Coutner 1 read/write
042h	Counter 2 read/write
043h	Control register write only

Configuration Registers

There are eleven configuration registers inside the SiS85C460. An indexing scheme is used to access all the registers. Port 22h is the index register and port 23h is the data register. The configuration registers are accessed by first writing the index to port 22h and immediately followed by a read or a write to port 23h. The index is reset after data access. Every data access to port 23h must be preceded by an index write to port 22h, even if the same register is being accessed. All the reserved bits should be set to zero for future compatibility purpose. The contents of the registers are listed as follows.

Configuration Registers

Register 50 (index50) Default = 00

bit 7, 6 **DRAM Speed** (See DRAM Speed Options on page 10)
00: Slowest
01: Slower
10: Faster
11: Fastest
Bit 7 also defines the cache read cycle time: 0/1 : 3T/2T

bit 5 **DRAM Write CAS Pulse Width**
0: 2T
1: 1T

bit 4~0 **DRAM Size Configuration**

	Bank-0	Bank-1	Bank-2	Bank-3	Total
00000	1M				1MB
00001	1M	1M			2MB
00010	1M	1M	2M		4MB
00011	1M	1M	4M		6MB
00100	1M	1M	2M	4M	8MB
00101	1M	1M	4M	4M	10MB
00110	1M	1M	16M		18MB
00111	2M				2MB
01000	2M	2M			4MB
01001	2M	4M			6MB
01010	2M	2M	4M		8MB
01011	2M	2M	4M	4M	12MB
01100	2M	16M			18MB
01101	2M	2M	16M		20MB
01110	2M	2M	4M	16M	24MB
01111	2M	2M	16M	16M	36MB
10000	4M				4MB
10001	4M	4M			8MB
10010	4M	4M	4M		12MB
10011	4M	4M	4M	4M	16MB
10100	4M	16M			20MB
10101	4M	4M	16M		24MB
10110	4M	16M	16M		36MB
10111	4M	4M	16M	16M	40MB
11000	8M				8MB
11001	8M	8M			16MB
11010	8M	8M	8M		24MB
11011	8M	8M	8M	8M	32MB
11100	16M				16MB
11101	16M	16M			32MB
11110	16M	16M	16M		48MB
11111	16M	16M	16M	16M	64MB

Note: 1MB = 256K x 36bits
2MB = 512K x 36bits
4MB = 1M x 36bits
8MB = 2M x 36bits
16MB = 4M x 36bits

Register 51 (index 51) Default = 00

bit 7 **Cache Enable**
0: Disable
1: Enable

bit 6 **Write Back Enable**
0: Disable (Write Through)
1: Enable (Write Back)

bit 5, 4 **Cache Size**
00: 32KB
01: 64KB
10: 128KB
11: 256KB and above

bit 3 **Cache Interleave Enable**
0: Disable
1: Enable

bit 2 **Cache On/Off**
0: Off
1: On

bit 1 **Cache Write Cycle**
0: 3T
1: 2T

bit 0 **Cache Burst Read Cycle (486 only)**
0: 1T
1: 2T
(Reserved and should be written with 1 in the 386 system)

Register 52 (index 52) Default = 00

bit 7 **Shadow RAM Read Enable**
0: Disable
1: Enable

bit 6 **Shadow RAM Write Protection Enable**
0: Disable
1: Enable

bit 5 **E8000h - EFFFFh Shadow RAM Enable**

bit 4 **E0000h - E7FFFh Shadow RAM Enable**

bit 3 **D8000h - DFFFFh Shadow RAM Enable**

bit 2 **D0000h - D7FFFh Shadow RAM Enable**

bit 1 **C8000h - CFFFFh Shadow RAM Enable**

bit 0 **C0000h - C7FFFh Shadow RAM Enable**

Register 53 (index 53) Default = 00

bit 7 **System BIOS ROM Size**
0: 64K
1: 128K

bit 6 **Combine System BIOS with C0000h~C7FFFh region for ROM area**
0: Disable
1: Enable

bit 5 **F0000h ~ FFFFFh Shadow RAM Cacheable**
0: Non-Cacheable
1: Cacheable

bit 4 **C0000h ~ C7FFFh Shadow RAM Cacheable**
0: Non-Cacheable
1: Cacheable

bit 3, 2 **DMA Cycle Up to 64MB Program A25 and A24**
bit 3: A25
bit 2: A24

bit 1 **Data Parity Check Enable**
0: Disable
1: Enable

bit 0 **De-turbo Switch Enable**
0: De-turbo Switch Enable
1: Always turbo, ignore the Status of Turbo Switch

Register 54 (index 54) Default = 00

bit 7 **Allocation of Non-cacheable Area #1**
0: Local DRAM
1: AT Bus, local DRAM disabled

bit 6~4 **Size of Non-Cacheable Area #1 (within 16MB)**
000: 0KB (disabled)
001: 64KB
010: 128KB
011: 256KB
100: 512KB
101: 1MB
110: 2MB
111: 4MB

bit 3 **Allocation of Non-Cacheable Area #2**
0: Local DRAM
1: AT Bus, local DRAM disabled

bit 2~0 **Size of Non-Cacheable Area #2 (within 64MB)**

000: 0KB (disabled)
001: 64KB
010: 128KB
011: 256KB
100: 512KB
101: 1MB
110: 2MB
111: 4MB

Register 55 (index 55) Default = 00

bit 7~0 **A23~A16 of Non-Cacheable Area #1 (within 16MB)**

Register 56 (index 56) Default = 00

bit 7~0 **A23~A16 of Non-Cacheable Area #2 (with 64MB)**

Register 57 (index 57) Default = 00

bit 7, 6 **A25 and A24 of Non-Cacheable Area #2**

bit 5 **Gate A20 Emulation Enable**
0: Disable
1: Enable

bit 4 **Fast Reset Emulation Enable**
0: Disable
1: Enable

bit 3 **Fast Reset Latency Control**
0: 2us
1: 6us

bit 2 **Slow Refresh Enable (1:4)**
0: Normal Refresh
1: Slow Refresh

bit 1 **De-turbo ON/OFF**
0: Turbo
1: De-Turbo

bit 0 **Cache Sizing Enable**
0: Normal operation
1: Always Cache hit

Register 58 (index 58) Default = 00

bit 7 **Slow CPU (below 25MHz) Enable**
0: Disable
1: Enable

bit 6 **DRAM Write Cycle**
0: 1 wait state
1: 0 wait state

bit 5 **Resvered and should be written with 1**

bit 4 **De-turbo Hold Time**

0: Hold 4us
1: Hold 8us (Every 12us)

bit 3 **Reserved and should be written with 0**

bit 2 **Combine System BIOS with C8000h~CFFFFh region for ROM area**

0: Disable
1: Enable

bit 1, 0 **Reserved and should be written with 0**

Register 60 (index 60) Default = 00

bit 7~5 **Bus Clock Frequency Selection**

000: BUSCLK = 7.159 MHZ
001: BUSCLK = 1/10 CLKIN
010: BUSCLK = 1/8 CLKIN
011: BUSCLK = 1/6 CLKIN
100: BUSCLK = 1/5 CLKIN
101: BUSCLK = 1/4 CLKIN
110: BUSCLK = 1/3 CLKIN
111: BUSCLK = 1/2 CLKIN

bit 4~0 **Reserved and should be written with 0**

Register 61 (index 61) Default = 01

bit 7, 6 **16-Bit I/O Cycle Command Recovery Time Selection**

00: 8 BUSCLK
01: 5 BUSCLK
10: 3 BUSCLK
11: 2 BUSCLK

bit 5, 4 **8-Bit I/O Cycle Command Recovery Time Selection**

00: 16 BUSCLK
01: 11 BUSCLK
10: 7 BUSCLK
11: 4 BUSCLK

bit 3 **Reserved and should be written with 1**

bit 2 **16-bit Memory, I/O Wait State Selection**

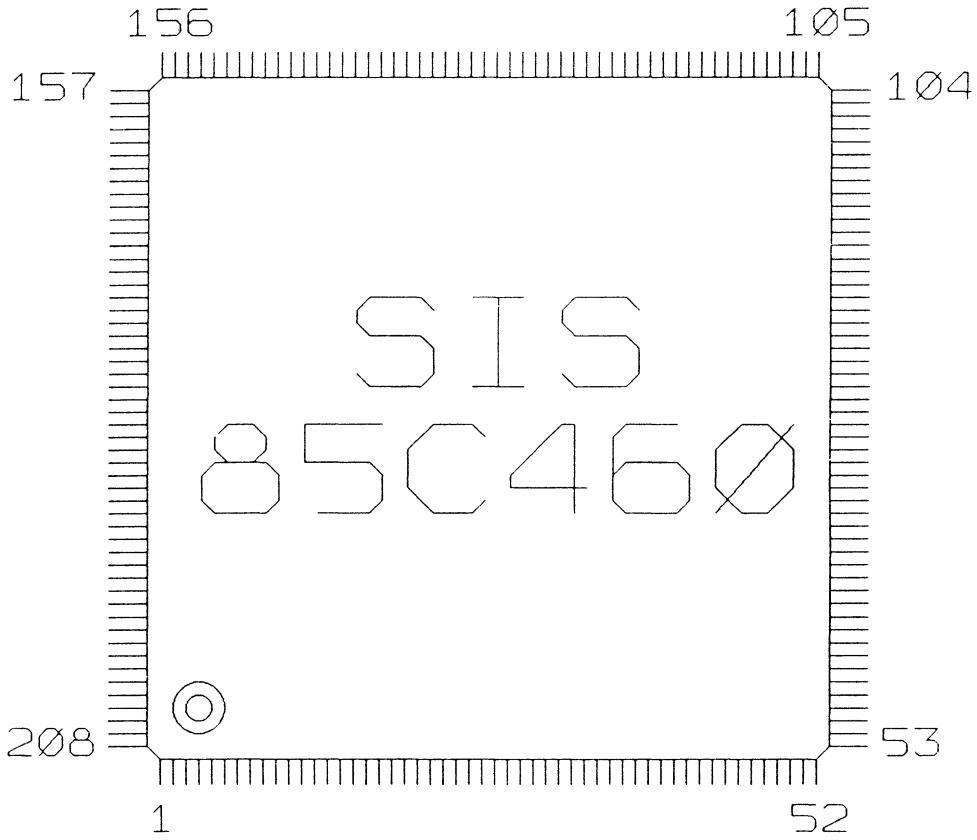
0: 2 wait states
1: 1 wait states

bit 1 **8-bit Memory, I/O Wait State Selection**

0: 5 wait states
1: 4 wait states

bit 0 **Reserved and should be written with 1**

PIN ASSIGNMENT



PIN ASSIGNMENT

1	CLKIN	53	SD11	105	IGNNE*[PREQ386]	157	CAS1*
2	14MHZ	54	GND	106	BLAST*[PREQ387]	158	CAS0*
3	IOR*	55	SD12	107	BRDY*[NC]	159	MA10
4	IOW*	56	SD13	108	BE3*	160	MA9
5	GND	57	SD14	109	BE2*	161	MA8
6	HDEN*	58	SD15	110	BE1*	162	MA7
7	LDEN*	59	GND	111	BE0*	163	MA6
8	BDIR	60	GND	112	NMI	164	GND
9	SDIR	61	VCC	113	INTR	165	VCC
10	VCC	62	PD1	114	VCC	166	MA5
11	ASRTC	63	A31	115	A20M*[CPUA20]	167	MA4
12	DSRTC*	64	A26	116	PCD[BZ387*]	168	MA3
13	DWRTC*	65	A25	117	SPK	169	MA2
14	CLKOUT	66	A24	118	PWRGD	170	MA1
15	GND	67	A23	119	GND	171	MA0
16	ZWS*	68	A22	120	LOCK*	172	BALE
17	XD0	69	A21	121	LBD*	173	AEN
18	XD1	70	A20	122	LRDY*	174	GND
19	XD2	71	A19	123	TA7/IRQ15	175	IORDY*
20	XD3	72	A18	124	TA6/IRQ14	176	EADS*[BZ386*]
21	XD4	73	A17	125	TA5/IRQ12	177	MPXS2/IRQ11
22	XD5	74	A16	126	TA4/IRQ7	178	MPXS1/IRQ10
23	XD6	75	GND	127	TA3/IRQ3	179	MPXS0/IRQ9
24	XD7	76	A15	128	TA2/DRQ7	180	MPXI2/IRQ8
25	PD0	77	A14	129	TA1/DRQ6	181	MPXI1/IRQ6
26	PD2	78	A13	130	TA0/DRQ5	182	MPXI0/IRQ5
27	D16	79	A12	131	TAWE*/WIRQ	183	MEMCS16*
28	D17	80	A11	132	ALT/DTURBO	184	IOCS16*
29	D18	81	A10	133	ALTWE*/RC*	185	MASTER*
30	D19	82	A9	134	MWE*	186	GND
31	D20	83	A8	135	GND	187	DACK7*
32	D21	84	A7	136	KWEX*	188	DACK6*
33	D22	85	A6	137	KWEY*	189	DACK5*
34	D23	86	A5	138	RAS3*	190	DACK3*
35	GND	87	A4	139	RAS2*	191	DACK2*
36	HOLD	88	KEN*[ERR386*]	140	RAS1*	192	DACK1*
37	BS16*	89	GND	141	RAS0*	193	DACK0*
38	GND	90	KBROMCS*	142	GND	194	GND
39	D24	91	A3	143	KREX*	195	TC
40	D25	92	A2	144	KREY*	196	BHE*
41	D26	93	RSTCPU	145	MRE*/IOCHK*	197	REF*
42	D27	94	CCLKIN	146	GND	198	SYSCLK
43	VCC	95	ADS*	147	VCC	199	RSTDRV
44	D28	96	GND	148	KCE3*/DRQ3	200	GND
45	D29	97	VCC	149	KCE2*/DRQ2	201	VCC
46	D30	98	CPURDY*	150	KCE1*/DRQ1	202	MEMR*
47	D31	99	GND	151	KCE0*/DRQ0	203	MEMW*
48	PD3	100	W/R*	152	KA3X/KA3/IRQ4	204	SMEMR*
49	GND	101	D/C*	153	KA3Y/KA2/IRQ1	205	SMEMW*
50	SD8	102	M/IO*	154	GND	206	GND
51	SD9	103	HLDA	155	CAS3*	207	SA1
52	SD10	104	FERR*[ERR387*]	156	CAS2*	208	SA0

Note: [xxx] for 386 mode
/xxx for non-cache mode

Pin Definition

Pin No.	Symbol	Type	Name and Function
95	ADS*	I	The *address status* input from CPU is an active low signal that indicates a valid bus cycle definition and address are available on the cycle definition lines and address bus.
102	M/IO*	I	*Memory I/O* Definition is an input for indicating an I/O cycle when low, and a memory cycle when high.
100	W/R*	I	*Write/Read* Definition is an input for indicating a read cycle when low, and a write cycle when high.
101	D/C*	I	*Data/control* Definition is an input for indicating a control cycle when low, and a data cycle when high.
98	CPURDY*	O	*CPU Ready* output indicates that the current bus cycle is complete and the CPU will terminate the current cycle.
36	HOLD	O	The bus *hold* request is used to request the control of the CPU bus. HLDA will be asserted by the CPU after completing the current bus cycle.
103	HLDA	I	*Hold acknowledge* comes from the CPU in response to a HOLD request. It is active high and remains driven during bus hold. HLDA indicates that the CPU has given the bus to another bus master.
112	NMI	O	*Non-maskable interrupt* is an active high signal to the CPU and is generated to invoke a non-maskable interrupt.
113	INTR	O	*Interrupt* goes high whenever a valid interrupt request is asserted. It interrupts the CPU, and is usually connected to the CPU's interrupt pin.
37	BS16*	O	*Bus Size 16* is an active low output. When actived, SiS85C460 initiates a memory, I/O, or interrupt acknowledge cycle (as qualified by the signals M/IO#, D/C#, and W/R#).

Pin Definiton (continued) **for 486 Mode**

Pin No.	Symbol	Type	Name and Function
115	A20M*	O	*A20 Mask* is the fast A20GATE output to the CPU. It remains high during power up of the CPU reset period, and will force A20 to go low when active.
88	KEN*	O	The 80486 CPU *cache enable* pin is used when the current cycle is cacheable to the internal cache of the 80486 CPU. It is an active low signal asserted by the SiS85C460 during cacheable cycle.
176	EADS*	O	*External address strobe* indicates that a valid external address has been driven onto the 80486 CPU address pins. This address will be used for the CPU to perform an intenal cache invalidation cycle.
104	FERR*	I	*Floating point error* from the 80486 CPU. It is driven active when a floating point error occurs.
105	IGNNE*	O	*Ignore numeric error* informs the 80486 CPU to ignore a numeric error.
106	BLAST*	I	The *burst last* signal indicates that the next time BRDY* is returned the burst bus cycle is complete.
107	BRDY*	I	*Burst ready* indicates that data presented is valid and is used for the 80486 CPU to sample the data during burst cycles.
116	PCD	I	*Page cache disable* pin reflects the state of the page attribute bits of the 80486 CPU.

Pin Definition (continued) **for 386 Mode**

Pin No.	Symbol	Type	Name and Function
115	CPUA20	I	*CPU Address A20* input.
88	ERR386*	O	*Error of 386 CPU* is an actived low output caused by ERR387. It is only active during CPU reset, and is inactive once reset is discontinued. Connect to 80386 ERROR input.
176	BZ386*	O	*Busy of 386 CPU* is an active low output caused by BZ387 input, and should be connected to 80386 BUSY input.
104	ERR387*	I	*Error of 387* is an active low input for indicating an error in the 387 cycle, and determining the presence of the 387 during CPU reset.
105	PREQ386	O	*Request of 386 CPU* is an active high output caused by PREQ387, and should be connected to 80386 PEREQ input.
106	PREQ387	I	*Request of 387* is an active high input from 80387 request output.
116	BZ387*	I	*Busy of 387* is an active low input from 80387 busy output.
107	NC		

Pin Definition (continued)

Pin No.	Symbol	Type	Name and Function
120	LOCK*	I	The bus *lock* pin indicates that the current bus cycle is locked. The CPU will not allow other system bus masters access to the system bus while it is asserted.
121	LBD*	I	*Local bus device* cycle input for indicating a local bus device cycle. It can be connected to the MCS* output of Weitek 3167/4167.
122	LRDY*	I	*Local bus device ready* is an active low input, indicating that current local bus cycle is finished. It can be connected to the RDYOUT output of Weitek 3167/4167.
111-108	BE0-3*	I	*Byte enable* determine the bytes to be accessed during CPU or DMA cycles. During CPU cycles, they are decoded to generate SA1, SA0, and BHE*. During DMA or Master cycles, the reverse action occurs.
92,91, 87-76, 74-6 64	A2,A3, A4-A15, A16-A26 A31	I/O	CPU *address lines*. They will drive output during CPU hold.
208	SA0	I/O	*AT bus address 0* outputs address 0 for AT bus during AT and DMA cycle, and input address 0 for Master cycle. It outputs LOW, during 16-bit DMA cycle.
207	SA1	I/O	*AT bus address 1* outputs address 1 in AT and DMA cycle, and inputs address 1 in Master cycle.
196	BHE*	I/O	*Byte high enable* signal indicates that the high byte has valid data on the 16-bit data bus. This signal is always an output except in Master mode.
202	MEMR*	I/O	*AT-bus memory read* command signal is an output pin during AT/DMA/refresh/cycle and is an input in MASTER cycles. It is used to retrieve the data from memory.

Pin Definition (continued)

Pin No.	Symbol	Type	Name and Function
203	MEMW*	I/O	*AT-bus memory write* command signal is an output pin during AT/DMA cycle and is an input in MASTER cycles. This active low signal writes data into the selected memory.
204	SMEMR*	O	*AT-bus memory read,* it instructs the memory devices to drive data onto the data bus. It is active only when the memory to be accessed is within the lowest 1MB.
205	SMEMW*	O	*AT-bus memory write,* it instructs the memory devices to store the data present on the data bus. It is active only when the memory to be accessed is within the lowest 1MB.
3	IOR*	I/O	*AT-bus I/O read* command signal is an output pin during AT or DMA cycle and is an input in other cycles. When low, it strobes an I/O device for placing data on the data bus.
4	IOW*	I/O	*AT-bus I/O write* command signal is an output pin during AT or DMA cycle and is an input in other cycles. When low, it strobes data on the data bus into a selected I/O device.
172	BALE	O	*Bus address latch enable* is used on the system board to latch valid address and memory decodes from the CPU.
183	MEMCS16*	I	*16-bit memory chip select* indicates a 16-bit memory transfer when low, and 8-bit memory transfer when high.
184	IOCS16*	I	*16-bit I/O chip select* indicates that the current AT bus cycle is a 16-bit I/O transfer when low, and an 8-bit I/O transfer when high.
16	ZWS*	I	*Zero wait state* is an active low signal. The system ignores the state of IORDY* and immediately terminates AT bus current cycle without additional wait state when it is low.

Pin Definition (continued)

Pin No.	Symbol	Type	Name and Function
175	IORDY	I	*I/O channel ready* is normally high and can be pulled low by the devices on the AT slot bus to lengthen memory or I/O cycles by adding wait states.
185	MASTER*	I	*Master** is an active low signal from AT bus. When active, it indicates that another bus master has already taken over the control of the whole system, the address and control outputs are all in a high-impedence state.
173	AEN	O	*Address Enable* is used to degate the CPU and other device from the I/O channel to allow DMA transfers to take place.
1	CLKIN	I	*Oscillator clock input.*
14	CLKOUT	O	*Clock ouptut* for CPU clock.
94	CCLKIN	I	*Clock input* provides single chip controller an internal clock.
198	SYSCLK	O	*Bus clock* is the system clock for the AT bus. The frequency of the AT bus clock is software programmable, see configuration register 60 for detail.
2	14MHZ	I	*14MHz* is an input of 14.318 MHz, generated by an external oscillator. It is used to be the base clock for the timer, and DMA controller.
118	PWRGD	I	*Power good* is a power on reset input and SiS85C460 accepts valid inputs when this pin is high.
93	RSTCPU	O	*Reset CPU* is an active high output to reset the CPU.
199	RSTDRV	O	*Reset driver* is an active high output for a system reset.
6	HDEN*	O	*High Byte data enable* signal enables the high byte buffer of the SD bus.

Pin Definition (continued)

Pin No.	Symbol	Type	Name and Funciton
7	LDEN*	O	*Low Byte data enable* signal enables the buffer of the XD bus.
8	BDIR	O	*Data Buffer Direction* controls the direction flow of the buffer between the high byte SD and D15~D8 and the direction flow of the buffer between the XD and D7~D0. HIGH sets the data path from D15~D8 (D7~D0) to SD (XD) bus, LOW sets the data path from SD (XD) bus to D15~D8 (D7~D0).
9	SDIR	O	*SD low byte Data Direction* controls the direction flow of the low byte buffer between SD and XD. HIGH sets the data path from XD to SD, LOW sets the data path from SD to XD.
179 178 177	MPXS0/IRQ9 MPXS1/IRQ10 MPXS2/IRQ11	O	*Multiplexer I/O* selection pins. In non-cache scheme, they work as "Interrupt Request" (input) pins.
182 181 180	MPXI0/IRQ5 MPXI1/IRQ6 MPXI2/IRQ8	I	*Multiplexer I/O* input pins. In non-cached scheme, they work as "Interrupt Request" pins.
193~190 189~187	DACK0~3 DACK5~7	O	*DMA acknowledge* notifies the individual peripherals when one has been granted a DMA cycle. The active polarity of these lines is programmable. Reset initializes them to active low. Because these signals are used internally for cascading the DMA channels and for DMA page register selection, these signals must be programmed to active low.
195	TC	O	*Terminal count* gives information concerning the completion of DMA services. A pulse is generated by the DMA controller when terminal count (TC) for any channel is reached, except for channel 0 in memory-to-memory mode. During memory-to-memory transfers TC will be output when the TC for channel 1 occurs. When a TC pulse occurs, the DMA controller will terminate the service, and if auto-initialize is enabled, the base registers will be written to the current registers of that channel. The mask bit and TC bit in the Status word will be set for the currently active channel unless the channel is programmed for auto-initialize. In that case, the mask bit remains clear.

Pin Definition (continued)

Pin No.	Symbol	Type	Name and Function
117	SPK	O	*Speaker* is the output for the speaker.
11	ASRTC	O	*Address strobe of real time clock* device to latch the address from XD bus when CPU accesses the RTC.
12	DSRTC*	O	*Data read strobe of real time clock* device to drive data onto the XD bus when CPU accesses the RTC.
13	DWRTC*	O	*Data write of real time clock* device to store the data presented on the XD bus when CPU accesses the RTC. This pin must be connected to the R/W of RTC.
90	KBROMCS*	O	*Keyboard controller 8042 or system ROM chip selection.*
197	REF*	I/O	*Refresh* to initiate a refresh cycle. This signal is an input in master mode, and an output in other cycle.
138~141	RAS3~0*	O	*DRAM row address strobe.*
155~158	CAS3~0*	O	*DRAM column address strobe.*
159~163 166~171	MA10~6 MA5~0	O	*DRAM row/column address lines.*
134	MWE*	O	*Memory write enable* is an active low output signal for DRAM write enable.
145	MRE*/IOCHK*	O	*Memory read enable* is an active low output signal for DRAM read enable. In non-cache scheme, it is used as "I/O channel check".
123,124 125 126 127	TA7,6/IRQ15,14 TA5/IRQ12 TA4/IRQ7 TA3/IRQ3	I/O	*Tag RAM data bus lines.* *Interrupt requests* is executed by raising an IRQ input low to high and holding it high until it is acknowledged (edge-triggered mode) or just a high level on an IRQ input (level-triggered mode). In non-cache scheme, they are defined as "Interrupt Request".

Pin Definition (continued)

Pin No.	Symbol	Type	Name and Function
128~130	TA2~0/DRQ7~5	I/O	Tag RAM data bus lines. In non-cache scheme, they are defined as "DMA Request".
131	TAWE*/WIRQ	O	*Tag RAM* write enable is an active low signal. In non-cache scheme, it is defined as "Weitek 3167/4167 interrupt request".
136	KWEX*	O	*Cache write enable* for even bank.
137	KWEY*	O	*Cache write enable* for odd bank.
143	KREX*	O	*Cache read enable* for even bank.
144	KREY*	O	*Cache read enable* for odd bank.
148~151	KCE3~0*/ DRQ3~DRQ0	O	*Cache enable* pins are active low signal, indicating that the corresponding byte is accessed. In non-cache scheme, they are defined as "DMA Request".
132	ALT/DTURBO	I/O	*Alter* bit of cache indicating that data line has been written into. In non-cache scheme, it is used as an DE-TURBO pin.
133	ALTWE*/RC*	O	*Alter bit write enable* is the write strobe to the alter RAM. This signal is active low when cache read miss or cache write hit occurs, and is used to update the ALT bit. In non-cache scheme, Reset input from Keyboard controller will cause the CPU to be reset when this signal is low.
153	KA3Y/KA2/IRQ1	O	*KA3Y-Cache address 3* for odd bank when Cache interleave mode is used. *KA2-Cache address 2* when Cache non-interleave mode is used. *IRQ1-Interrupt requests* IRQ1 when non-Cache mode is used.
152	KA3X/KA3/IRQ4	O	*KA3X-Cache address 3* for even bank when Cache interleave mode is used. *KA3-Cache address 3* when Cache non-interleave mode is used. *IRQ4-Interrupt requests* IRQ4 when non-Cache mode is used.

Pin Definition (continued)

Pin No.	Symbol	Type	Name and Function
25,62, 26,48	PD0~3	I/O	*DRAM parity bits* generate parity bits in memory write cycle and accept parity bits in memory read cycle.
17~24	XD0~7	I/O	*Peripheral data bus* lines.
50~53 55~58	SD8~11 SD12~15	I/O	*Data bus* for the I/O devices.
27~34 39~42 44~47	D16~23 D24~27 D28~31	I/O	*Data bus* for the microprocessor, Memory, and I/O devices.
10,43, 61,97, 114,147, 165,201	VCC		*+5V DC Power*
5,15,35, 38,49,54, 59,60,75, 89,96,99, 119,135, 142,146, 154,164, 174,186, 194,200, 206	GND		*Ground*

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Min	Max	Unit
Ambient operating temperature	0	70	°C
Storage temperature	-40	125	°C
Input voltage	-0.3	5.5	V
Output voltage	-0.5	5.5	V

Note:

Stress above these listed may cause permanent damage to device. Functional operation of this device should be restricted to the conditions described under operating conditions.

DC Characteristics

T_A = 0 - 70 °C, V_{DD} = 5 V ± 5 % , GND = 0 V

Symbol	Parameter	Min	Max	Unit	Condition
V_{IL}	Input low voltage	-0.5	0.8	V	
V_{IH}	Input high voltage	2.0	VDD+0.5	V	
V_{OL}	Output low voltage	-	0.45	V	I_{OL} = 4.0 mA
V_{OH}	Output high voltage	2.4	-	V	I_{OH} = - 1.0 mA
I_{IL}	Input leakage current	-	±10	uA	$0 < V_{IN} < V_{DD}$
I_{OZ}	Tristate leakage current	-	±20	uA	$0.45 < V_{OUT} < V_{DD}$

AC Characteristics

T_A = 0 - 70 °C, V_{DD} = 5V ± 5%, V_{SS} = 0 V, C_L = 85/50* pF

Symbol	Parameter	Min	Typ	Max	Unit
T1	KCE* active delay*	3	7	12	ns
T2	KCE* inactive delay*	3	7	12	ns
T3	Tag address input setup time	8			ns
T4	BRDY* active delay*	3	8	14	ns
T5	BRDY* inactive delay*	3	6	10	ns
T6	BLAST* setup time	4			
T7	KEN* valid delay*	3	8	14	ns
T8	Cache Interleave KRE* active delay	3	7	11	ns
T9	Cache Interleave KRE* inactive delay	3	6	10	ns
T10	KA3X valid delay	3	9	14	ns
T11	KA3Y/KA2 valid delay	3	9	15	ns
T12	Cache Non-interleave KRE* active delay	3	9	15	ns
T13	Cache Non-interleave KRE* inactive delay	3	8	14	ns
T14	ADS* setup time	2			ns
T15	KWE* active delay	3	7	12	ns
T16	KWE* inactive delay	3	7	11	ns
T17	RDY* active delay	4	12	19	ns
T18	RDY* inactive delay	4	11	18	ns
T19	Tag address output valid delay	5	14	24	ns
T20	Tag address output floating delay	5	13	22	ns
T21	TAWE* active delay	4	12	20	ns
T22	TAWE* inactive delay	4	12	20	ns
T23	ALTWE* active delay*	4	11	17	ns
T24	ALTWE* inactive delay*	3	10	16	ns
T25	MRE* active delay	6	16	25	ns
T26	MRE* inactive delay	4	14	24	ns
T27	RAS* active delay	4	10	18	ns
T28	CAS* active delay	4	10	18	ns
T29	CAS* inactive delay	3	9	16	ns
T30	Column address valid delay	4	12	20	ns
T31	MWE* active delay	4	12	20	ns
T32	MWE* inactive delay	3	9	14	ns
T33	LBDY* setup time	4			ns
T34	LBCS* setup time	4			ns
T35	LBCS* hold Time	5			ns

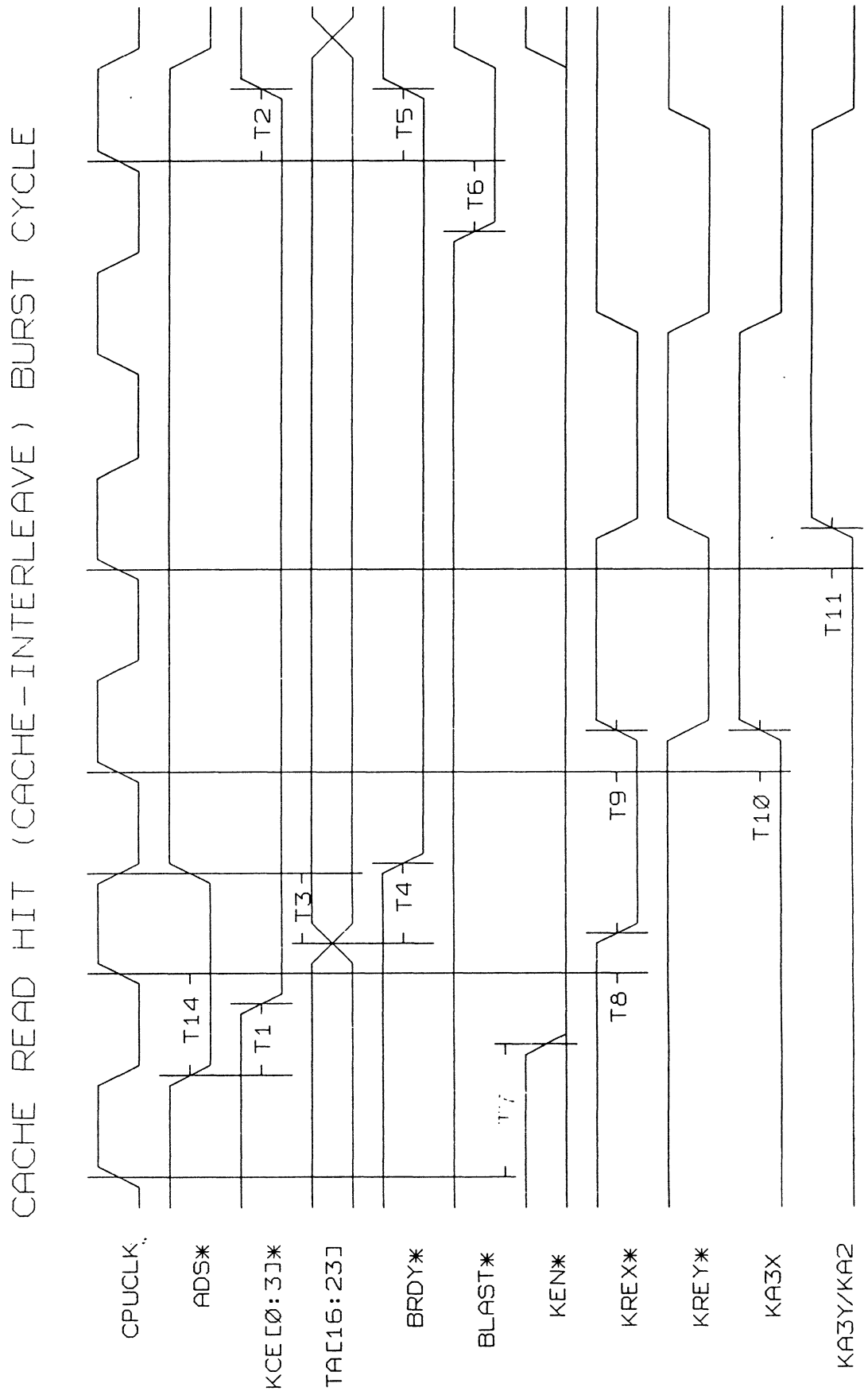
AC Characteristics (continued)

Symbol	Parameter	Min	Typ	Max	Unit
T36	RDY* from local bus setup time	4			ns
T37	RDY* from local bus hold time	5			ns
T38	RAS* inactive delay	4	9	16	ns
T39	Row Address valid delay	4	12	20	ns
T40	Fast cache write RDY* active delay	4	11	19	ns
T41	ALE active delay from SYSCLK falling	5	11	22	ns
T42	ALE inactive delay from SYSCLK	9	21	39	ns
T43	MEMCS16* set up time to SYSCLK	0			
T44	MEMCS16* hold time to SYSCLK	7			ns
T45	IOCS16* set up time to SYSCLK	4			ns
T46	IOCS16* hold time to SYSCLK	3			ns
T47	Command active delay from SYSCLK	8	16	29	ns
T48	Command inactive delay from SYSCLK	7	15	27	ns
T49	ZWS* set up time to SYSCLK	4			ns
T50	ZWS* hold time from SYSCLK	5			ns
T51	HDEN* active delay from BS16*	2	4	7	ns
T52	HDEN* inactive delay from BS16*	8	15	30	ns
T53	SDIR, BDIR active delay from BS16*	5	12	22	ns
T54	SDIR, BDIR inactive delay from BS16*	3	7	13	ns
T55	Data conversion SA0 delay from SYSCLK	6	14	26	ns
T56	Data conversion SA0 delay from SYSCLK	10	23	43	ns
T57	Address bus valid delay from REF*	5	12	22	ns
T58	Address bus float delay from REF*	7	23	44	ns
T59	Address set up time to IOR*, IOW* active	16			ns
T60	Address hold time from IOR*, IOW* inactive	0			ns
T61	SDIR,BDIR delay from command active	8	18	33	ns
T62	SDIR,BDIR delay from command inactive	20	45	84	ns
T63	SDEN*,HDEN* delay from command active	8	19	36	ns
T64	SDEN*,HDEN* delay from command inactive	20	19	36	ns
T65	Data active delay form BS16*	3	7	12	ns
T66	Data valid delay from SYSCLK	19	21	39	ns
T67	Data float delay from BS16*	3	7	12	ns
T68	D15-0 data set up time to command inactive	15			ns
T69	D15-0 data hold time to command inactive	8			ns
T70	D7-0 data valid delay from SYSCLK	10	18	30	ns
T71	D15-8 data valid delay from SYSCLK	7	16	26	ns
T72	D23-16 data valid dealy from SYSCLK	8	20	39	ns
T73	D31-24 data valid delay from SYSCLK	16	38	48	ns
T74	D15-0 data valid delay from D31-16 valid	9	15	27	ns
T75	D7-0 data valid delay from D31-24 valid	15	35	65	ns
T76	D7-0 data valid delay from D23-16 valid	6	14	26	ns
T77	D7-0 data valid delay from D15-8 valid	9	13	39	ns
T78	Data active delay from command active	16	29	54	ns
T79	Data float dealy from command inactive	10	15	28	ns

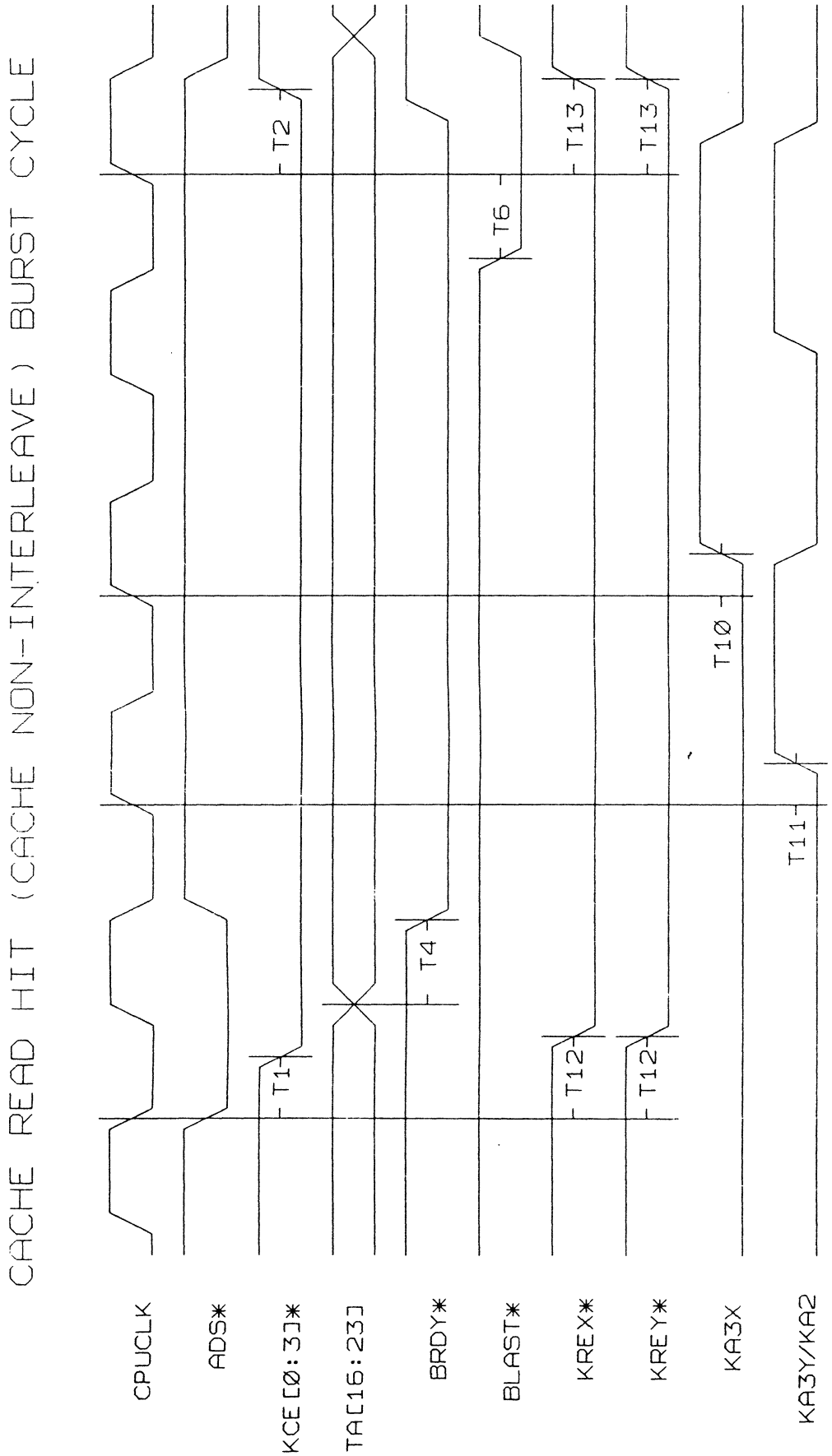
AC Characteristics (continued)

Symbol	Parameter	Min	Typ	Max	Unit
T80	DMA clock delay form bus clock			8	ns
T81	Low byte address valid delay			50	ns
T82	Low byte address invalid delay			45	ns
T83	Page address valid delay			60	ns
T84	Page address invalid delay			47	ns
T85	DACKn* active delay			41	ns
T86	DACKn* inactive delay			34	ns
T87	IOR* or MEMR* active delay			30	ns
T88	IOR* or MEMR* inactive delay			36	ns
T89	IOR* or MEMR* hold time	0			ns
T90	IOW* or MEMW* active delay			32	ns
T91	IOW* or MEMW* inactive delay			31	ns
T92	TC active delay			30	ns
T93	TC inactive delay			42	ns
T94	RSTDRV active delay	4	9	16	ns
T95	RSTDRV inactive delay	6	15	26	ns
T96	RSTCPU active delay*	2	6	11	ns
T97	RSTCPU inactive delay*	3	7	12	ns
T98	RSTCPU duration	25			CCLKIN

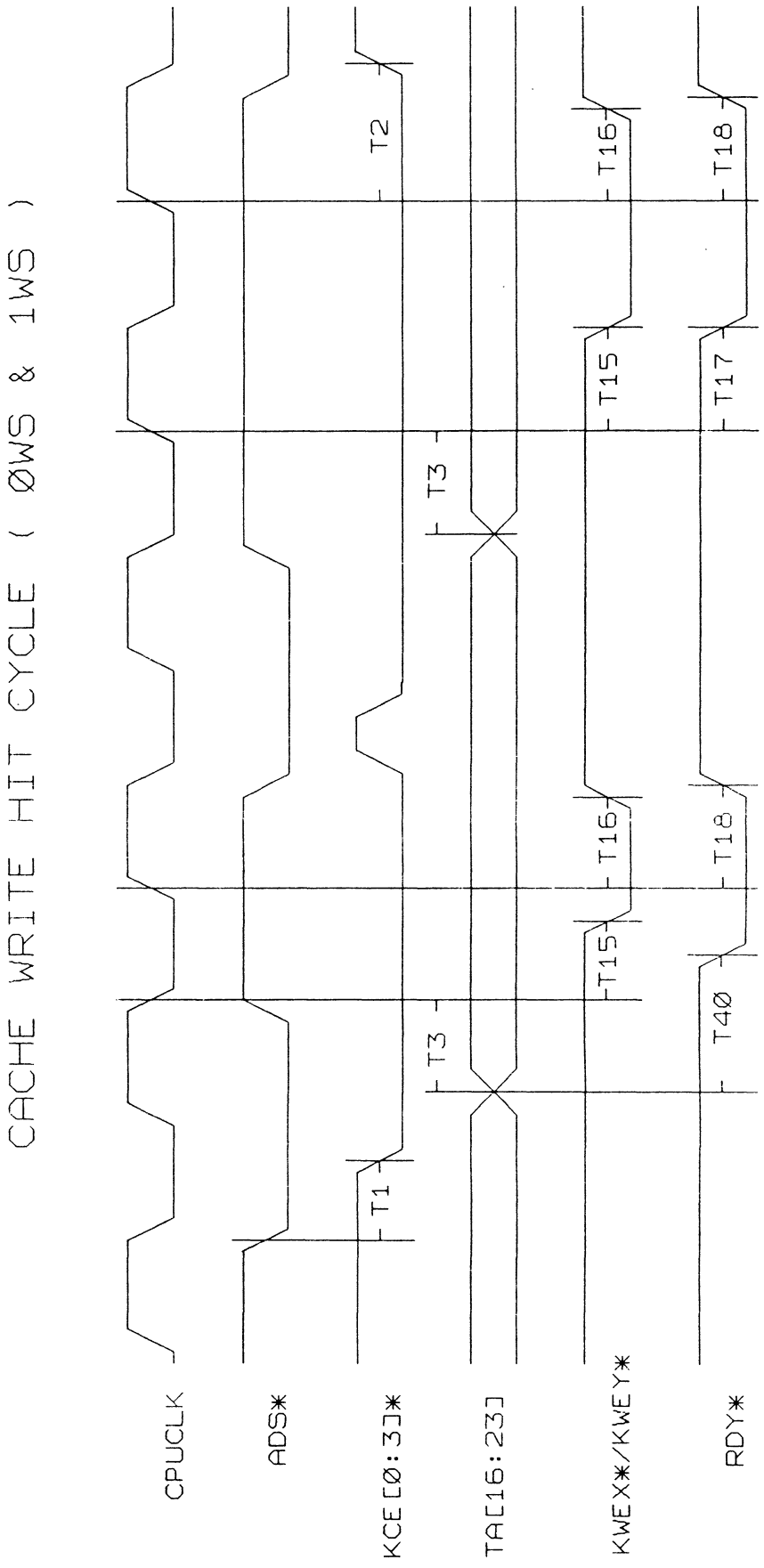
Timing Diagram for 486 Mode



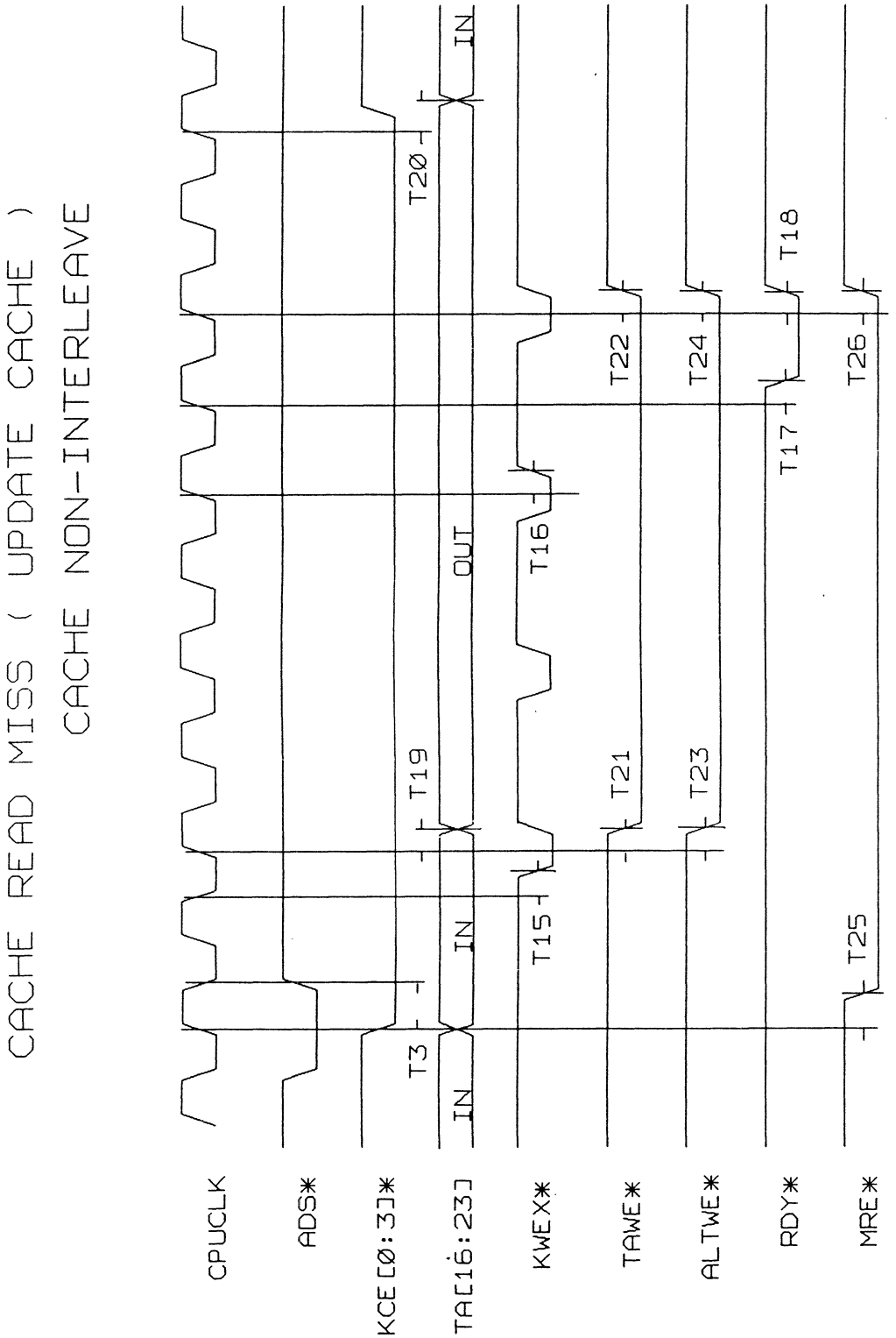
Timing Diagram for 486 Mode



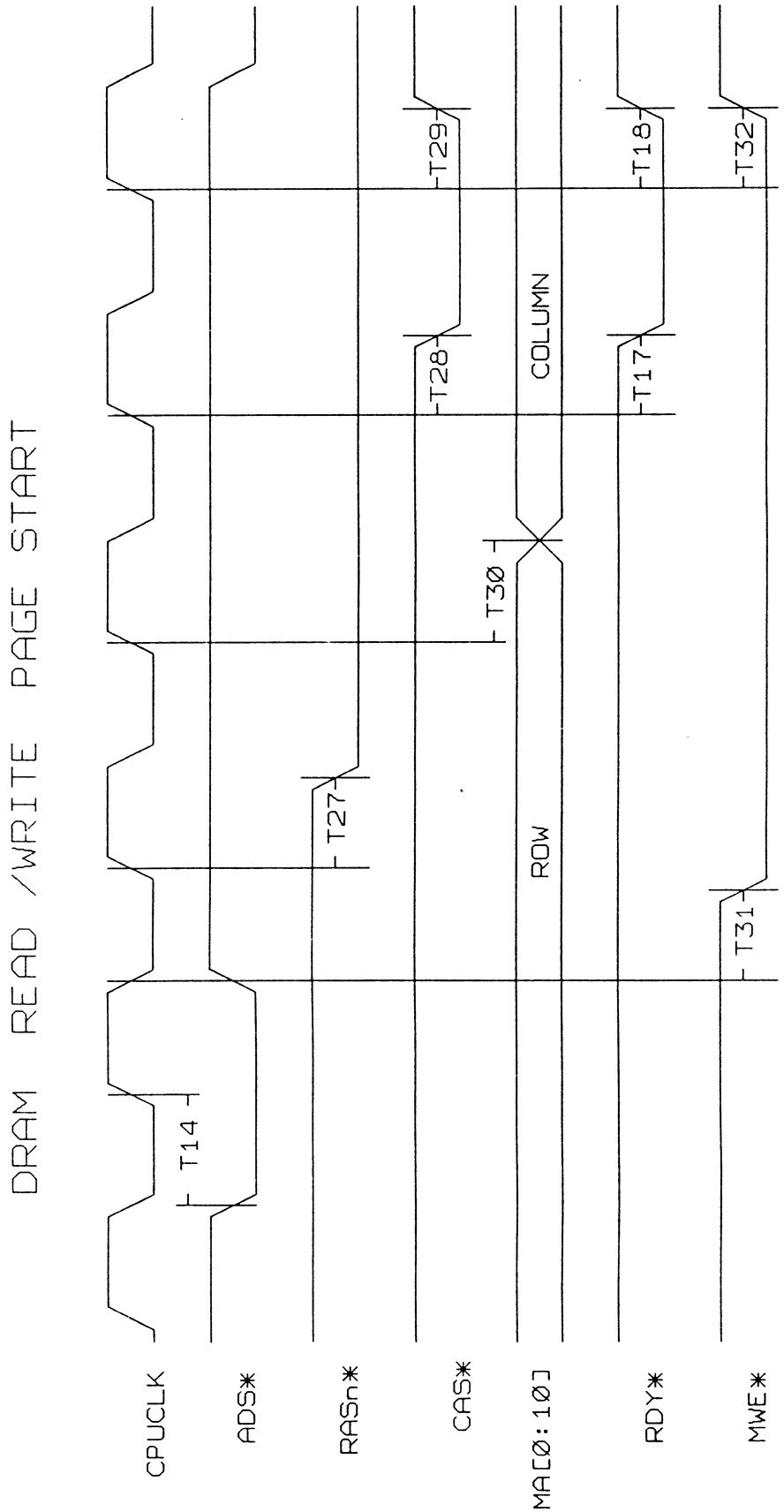
Timing Diagram for 486 Mode



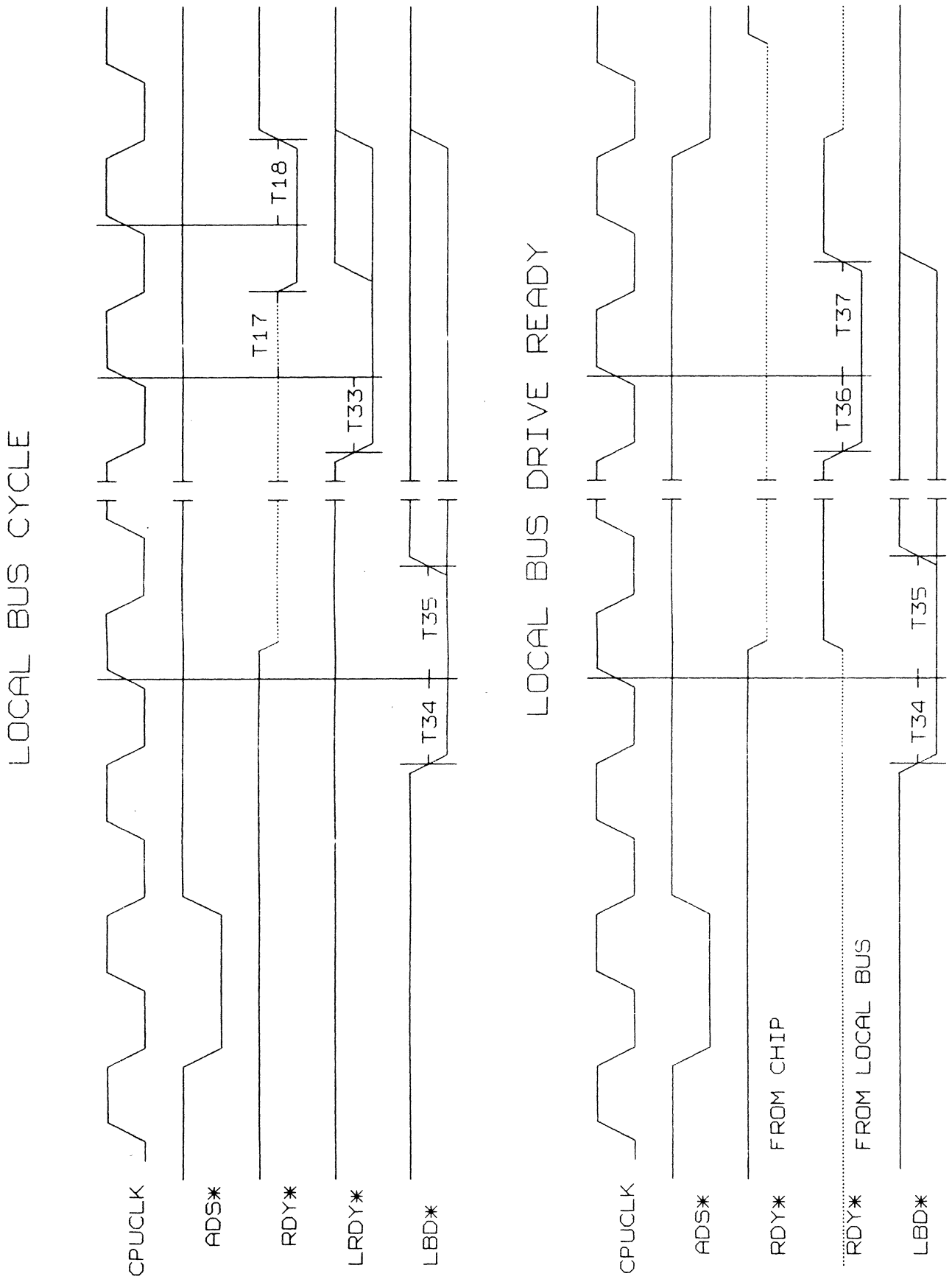
Timing Diagram for 486 Mode



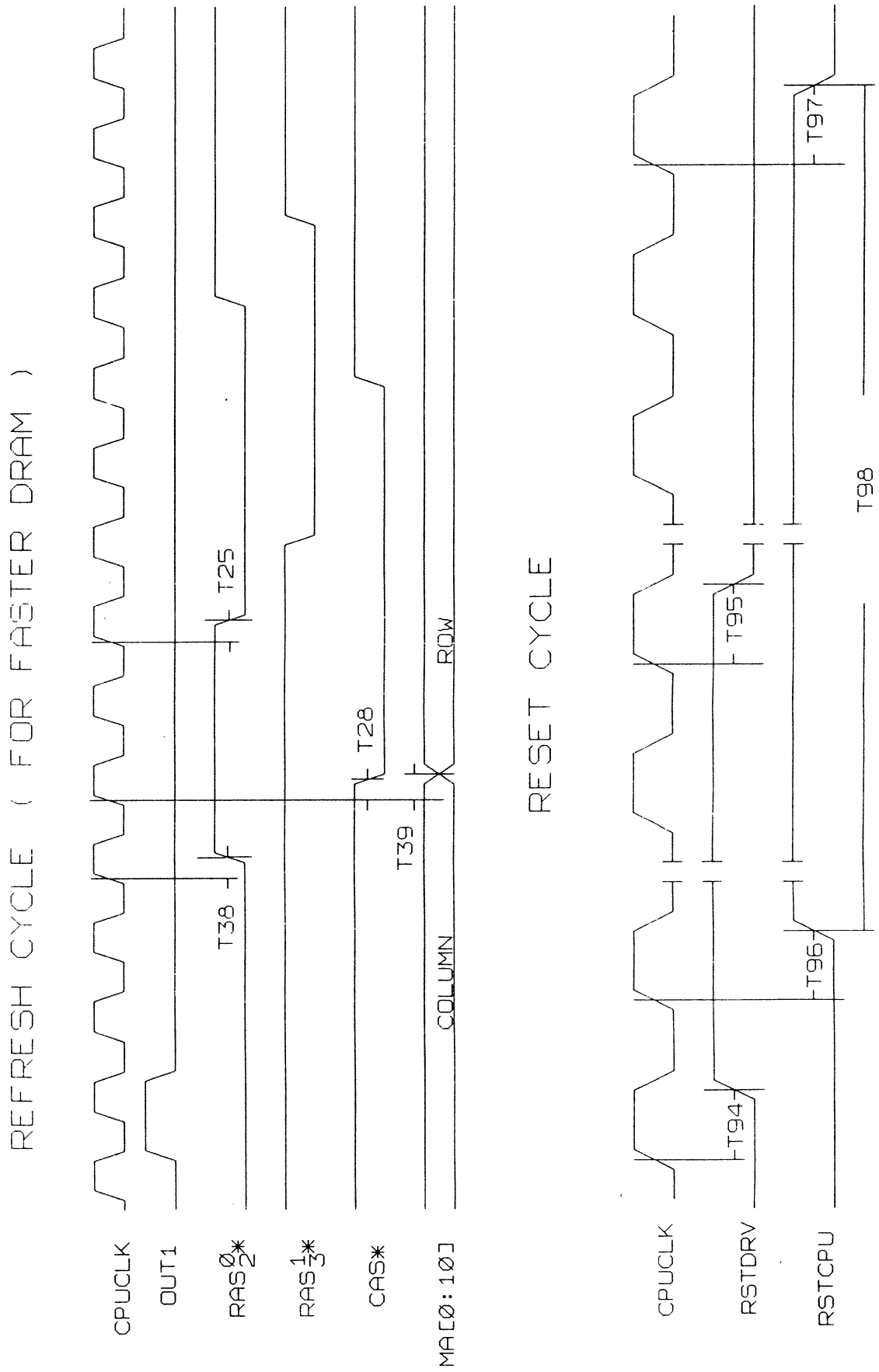
Timing Diagram for 486 Mode



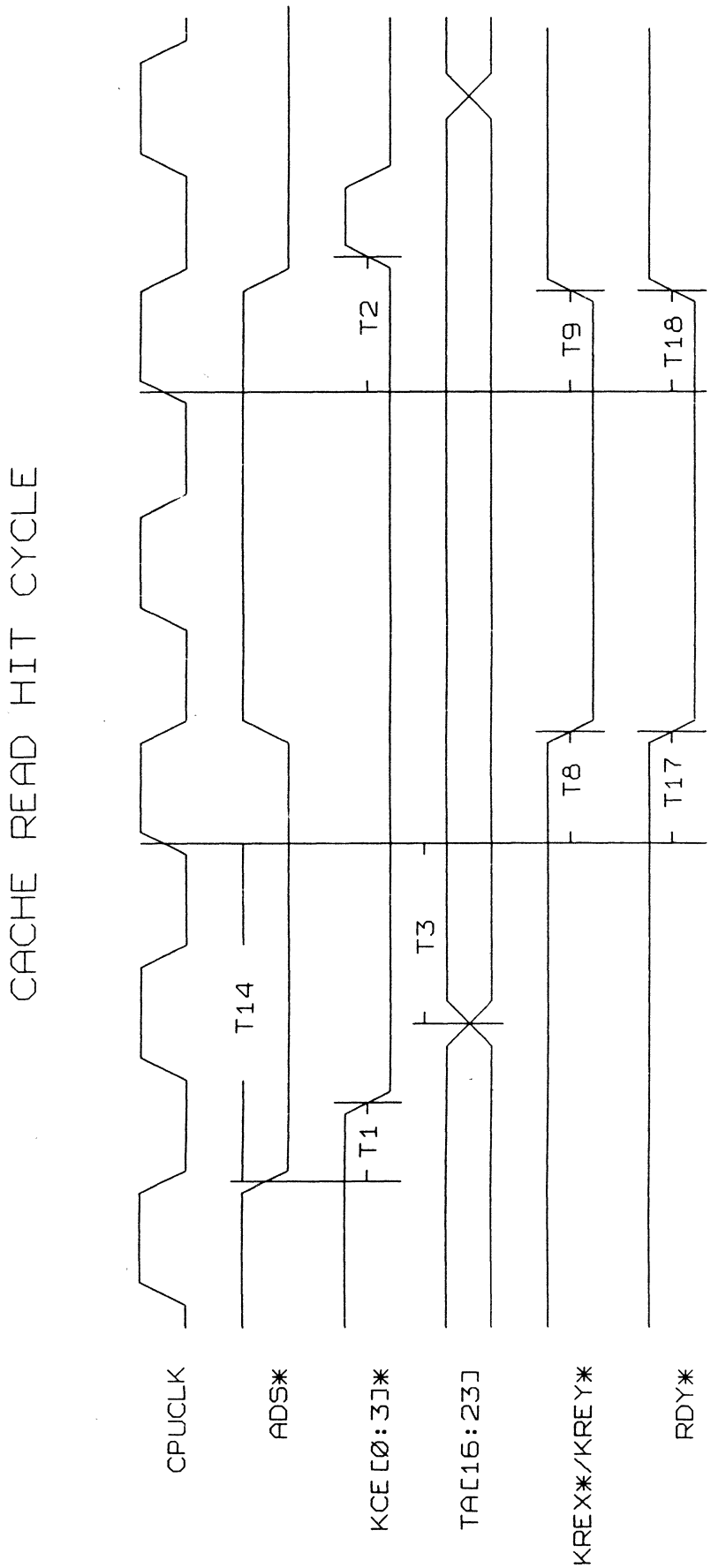
Timing Diagram for 486 Mode



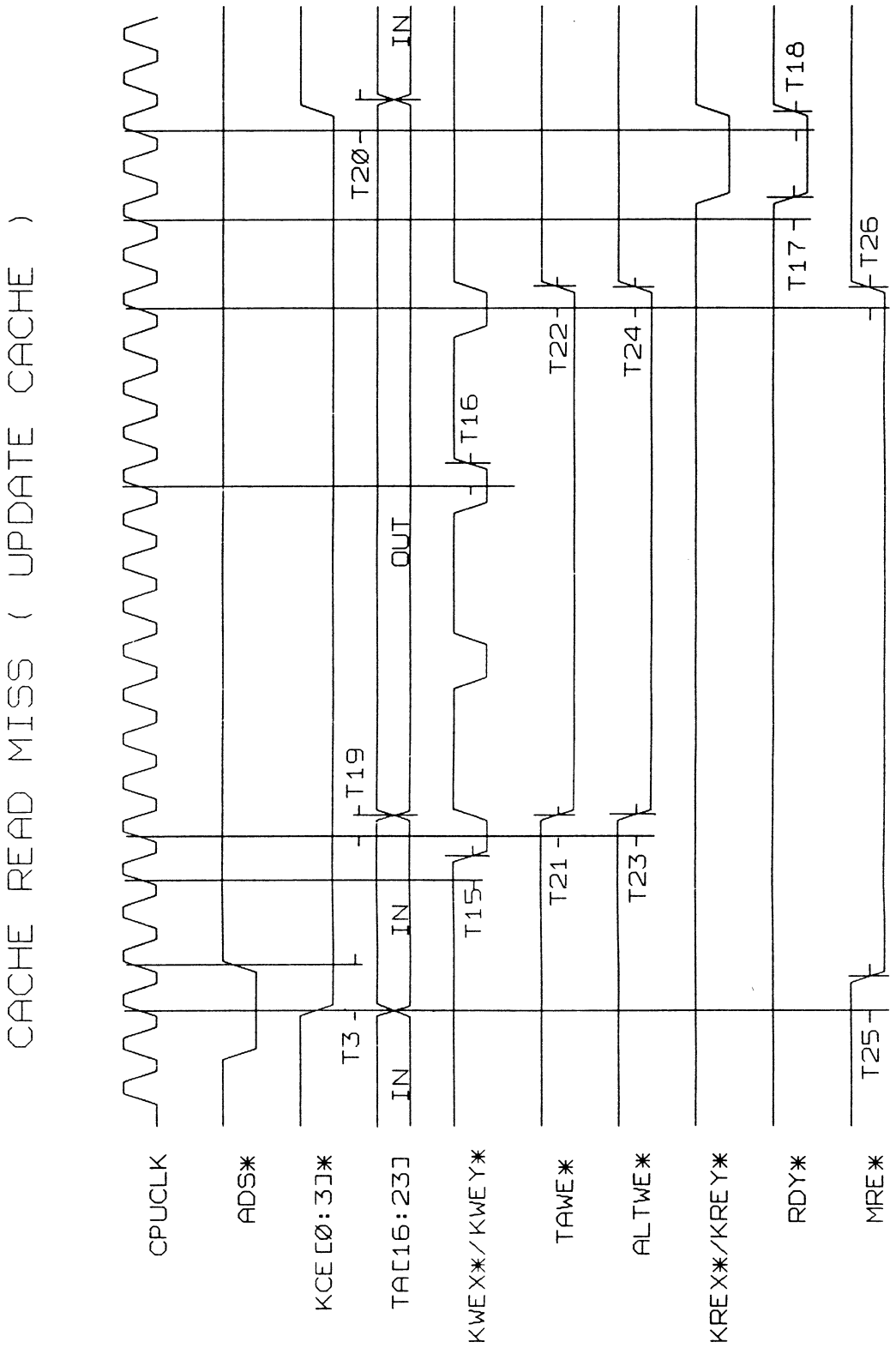
Timing Diagram for 486 Mode



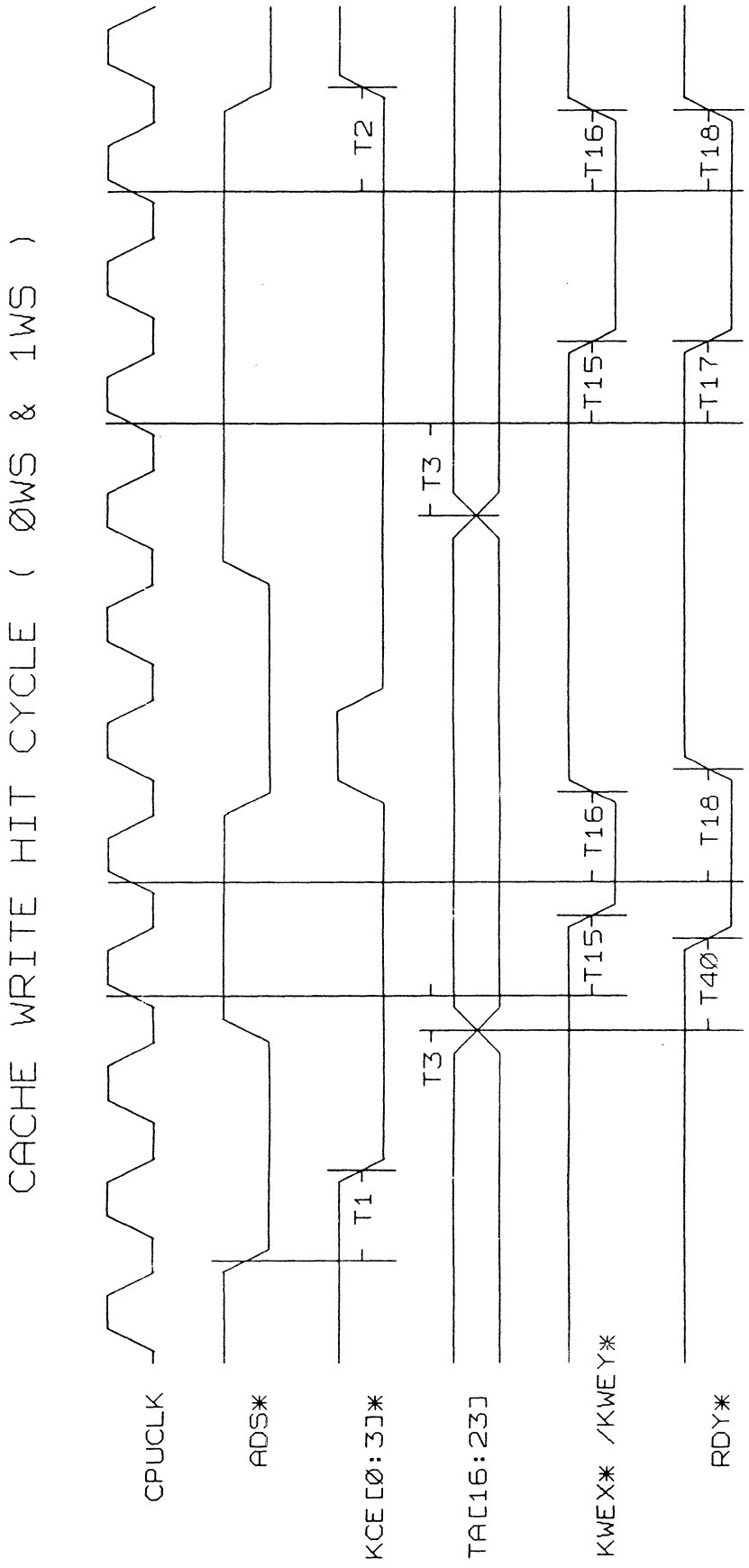
Timing Diagram for 386 Mode



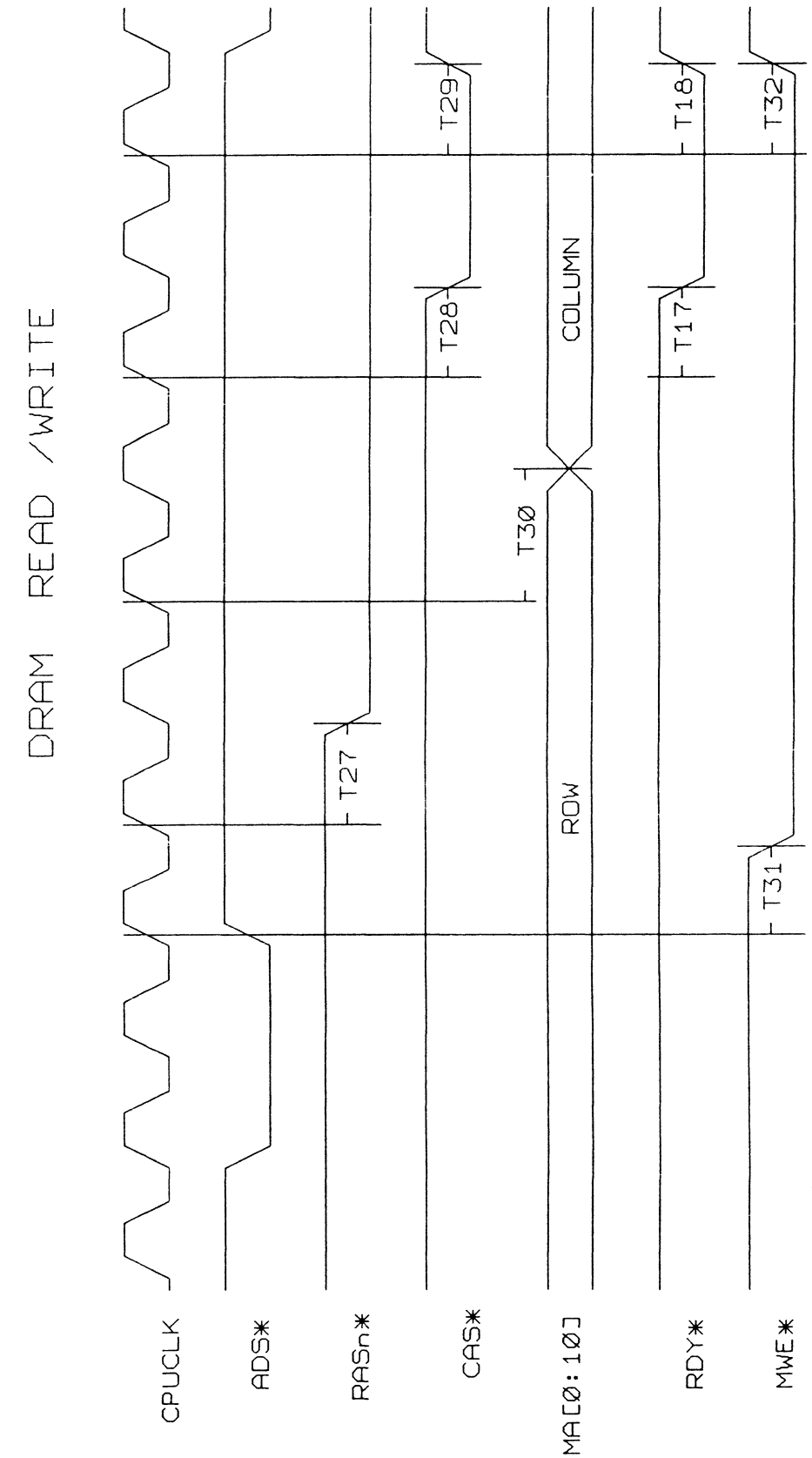
Timing Diagram for 386 Mode



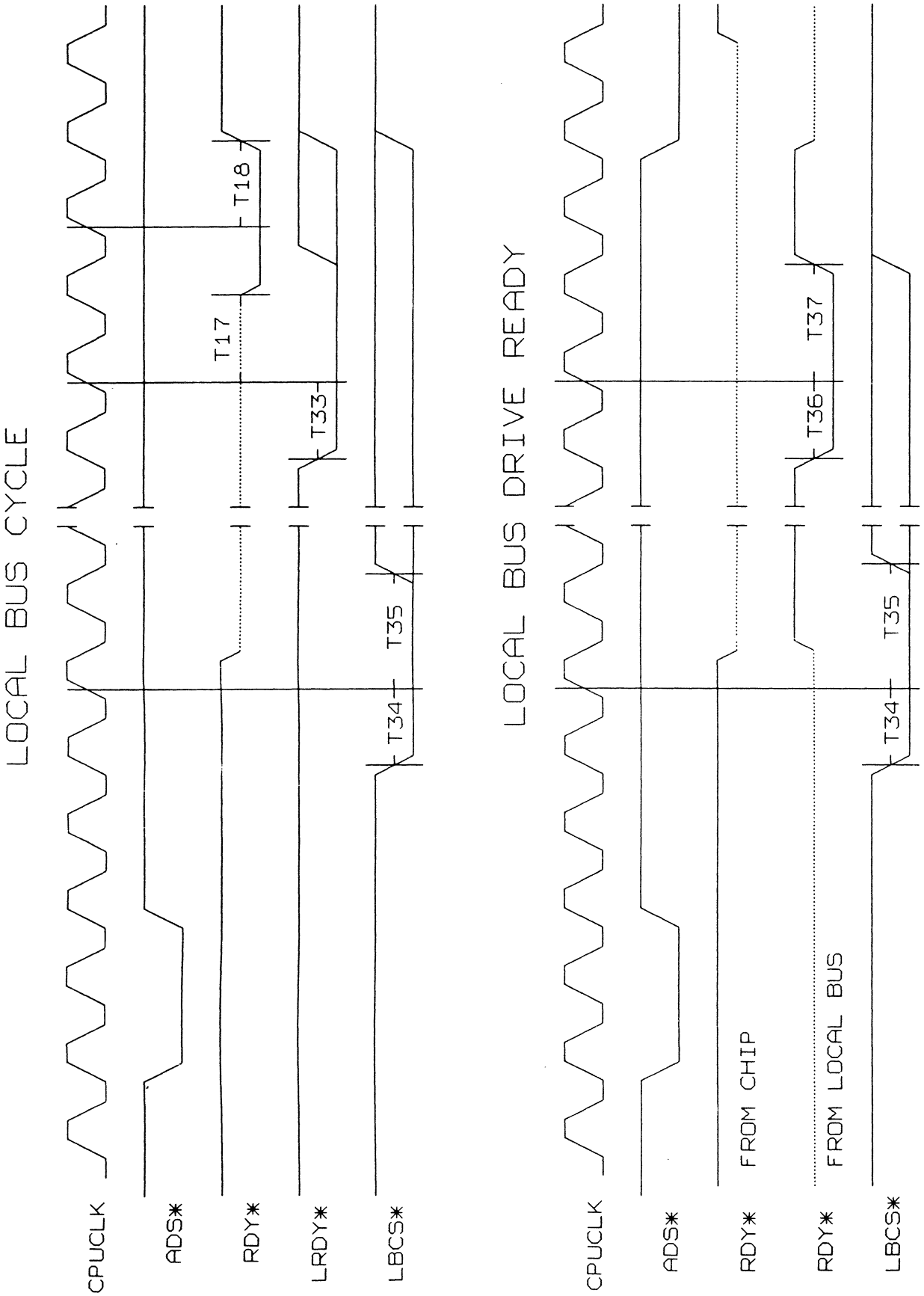
Timing Diagram for 386 Mode

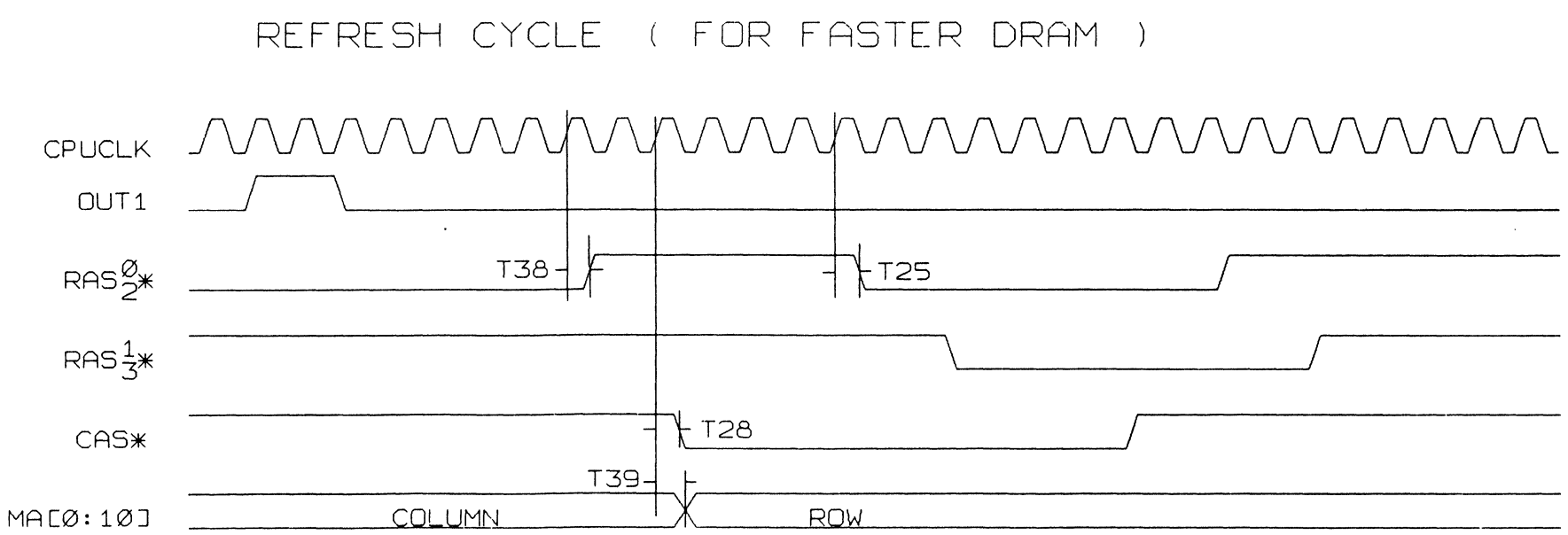


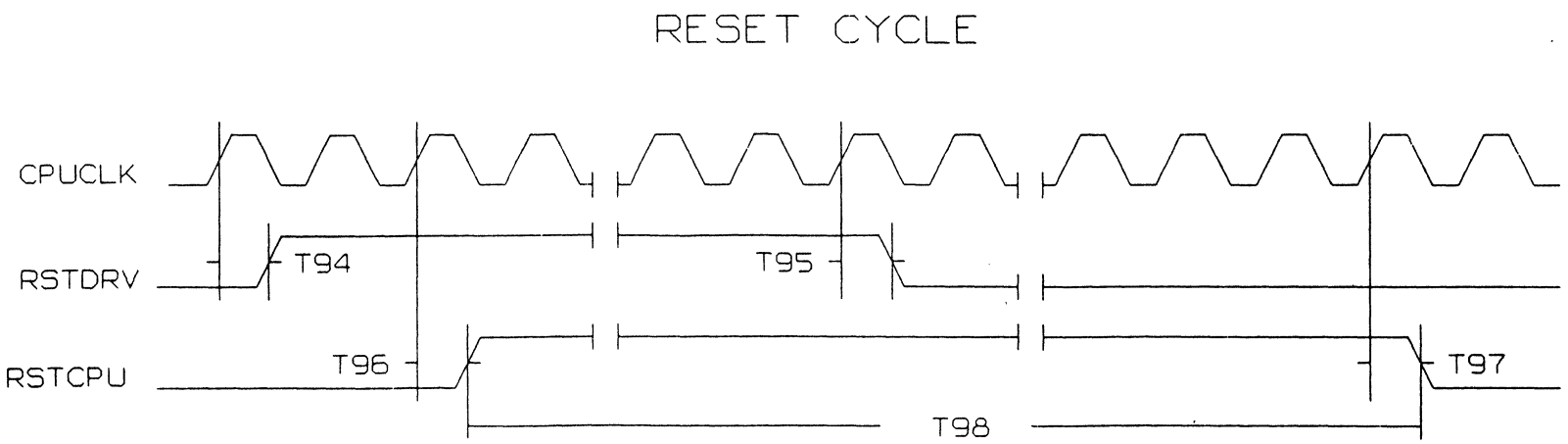
Timing Diagram for 386 Mode



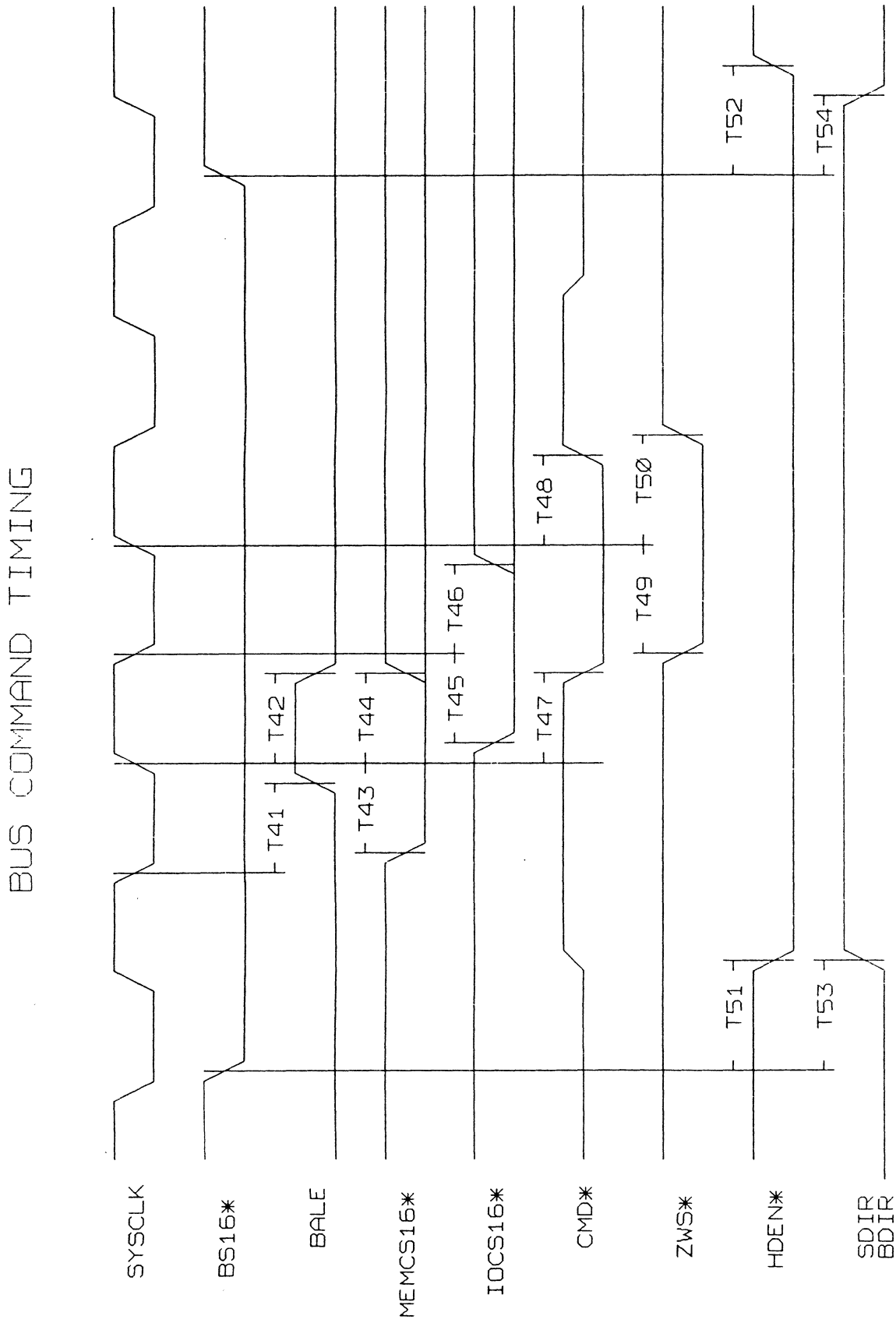
Timing Diagram for 386 Mode



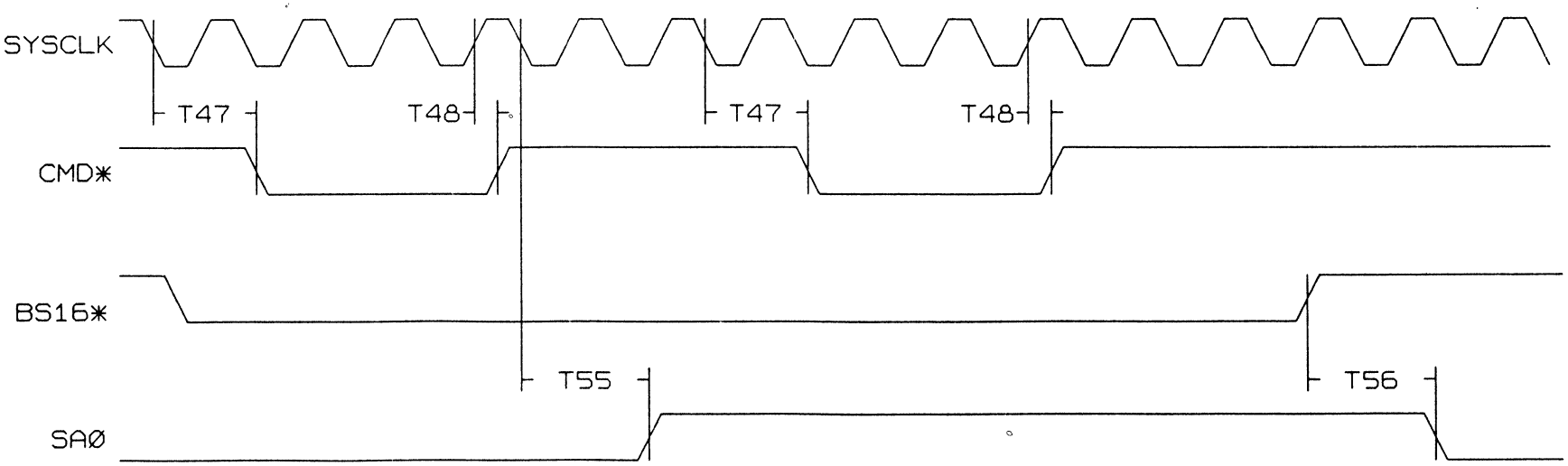

REFRESH CYCLE (FOR FASTER DRAM)
CPUCLK
OUT1
RAS Ø/2*
RAS 1/3*
CAS*
MA[Ø:1Ø]
T38
T25
T28
T39
COLUMN
ROW


RESET CYCLE
CPUCLK
RSTDRV
RSTCPU
T94
T95
T96
T97
T98

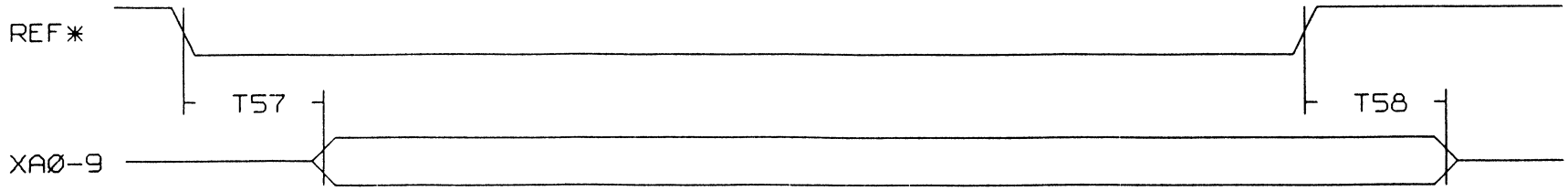
Timing Diagram



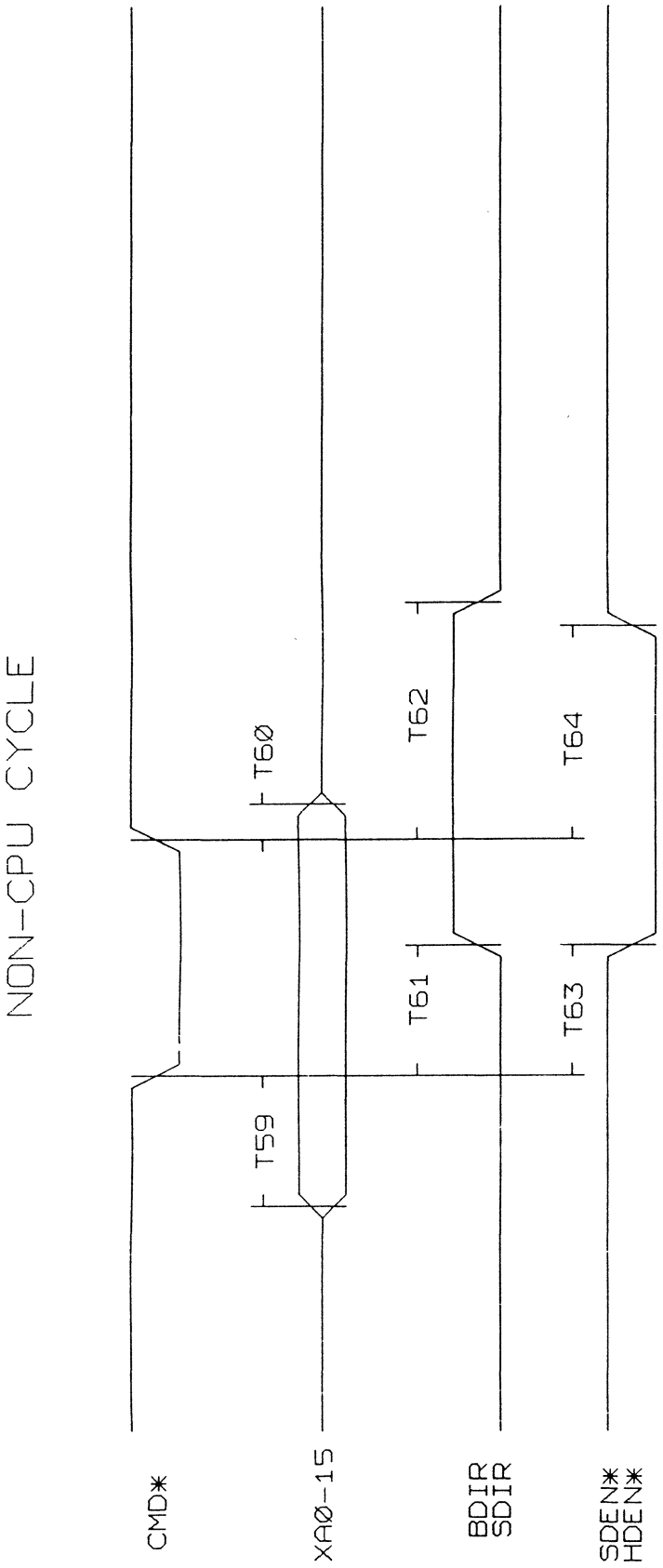
DATA CONVERSION CYCLE



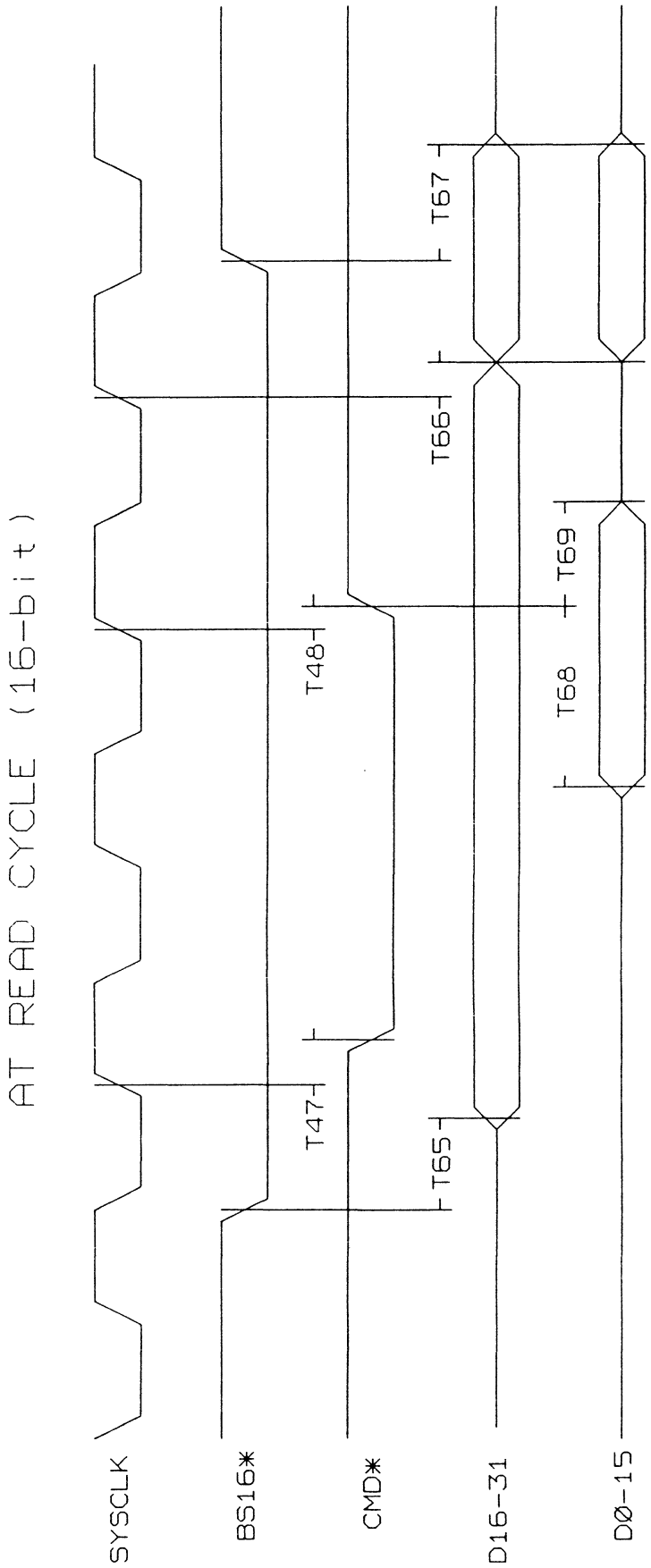
REFRESH CYCLE



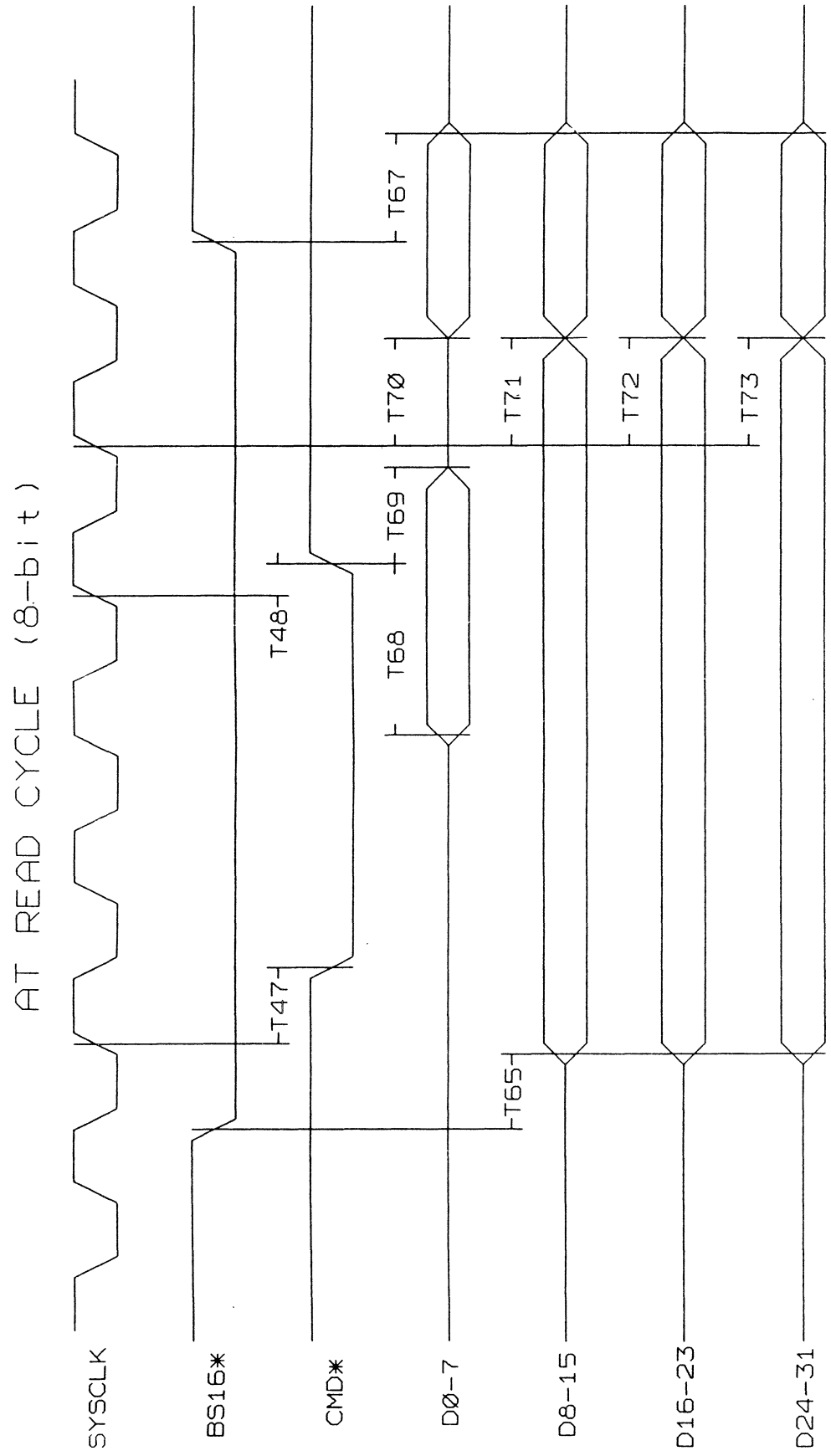
Timing Diagram



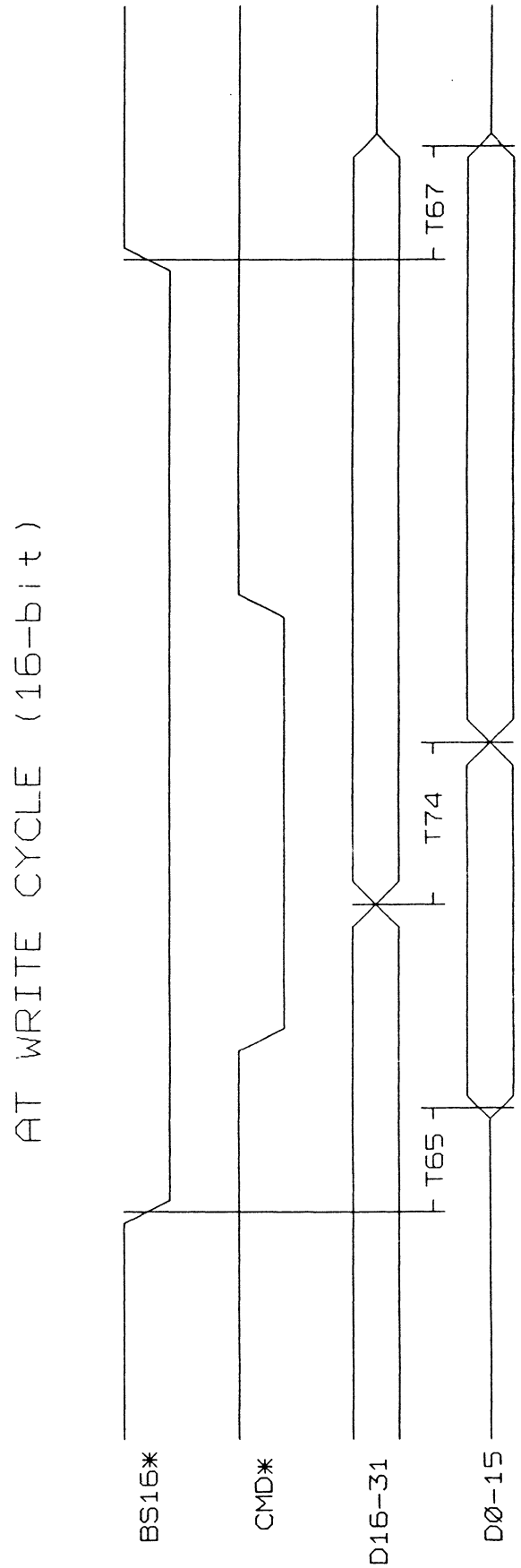
Timing Diagram



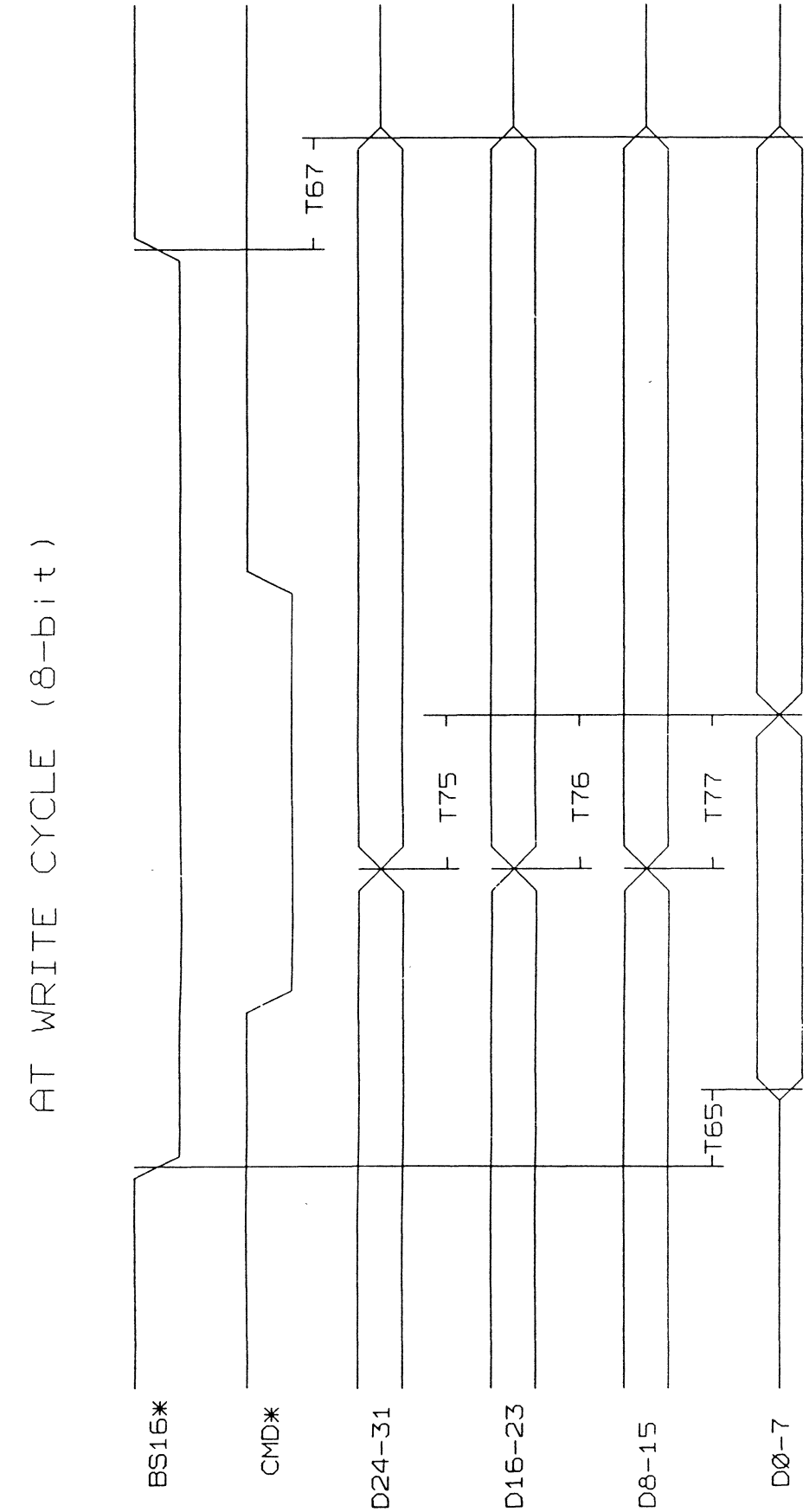
Timing Diagram



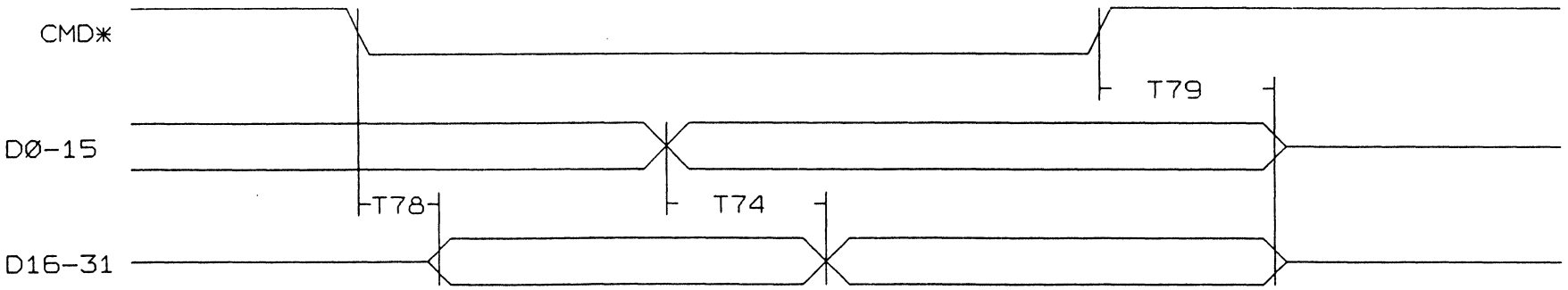
Timing Diagram



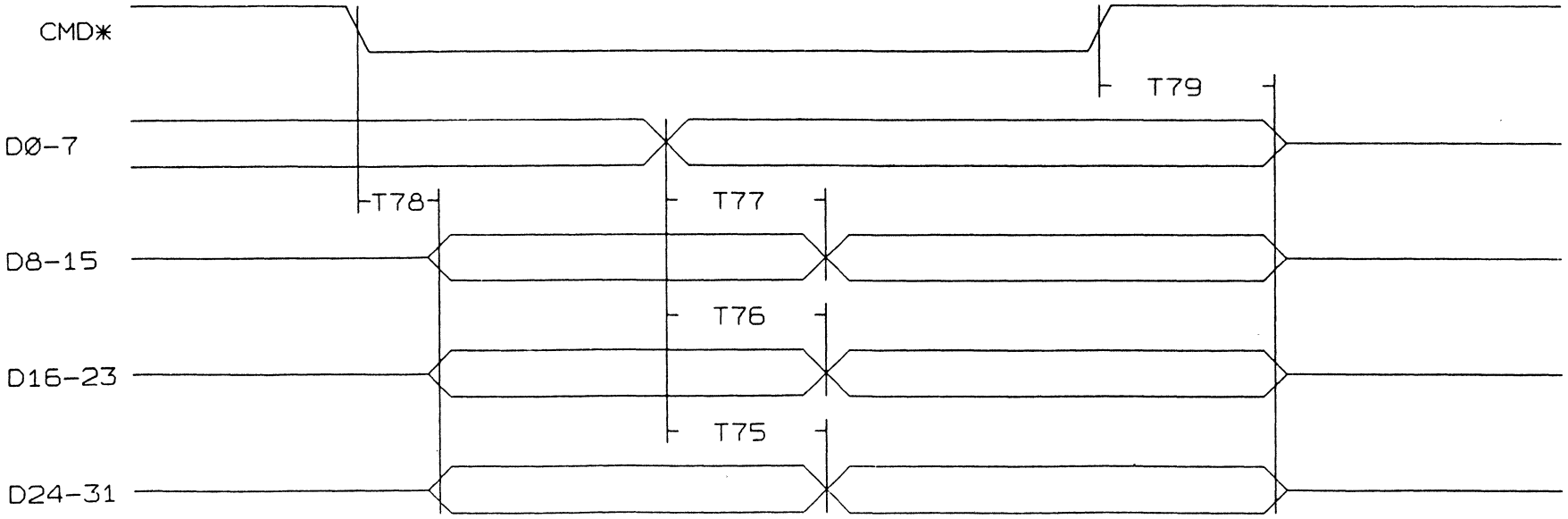
Timing Diagram



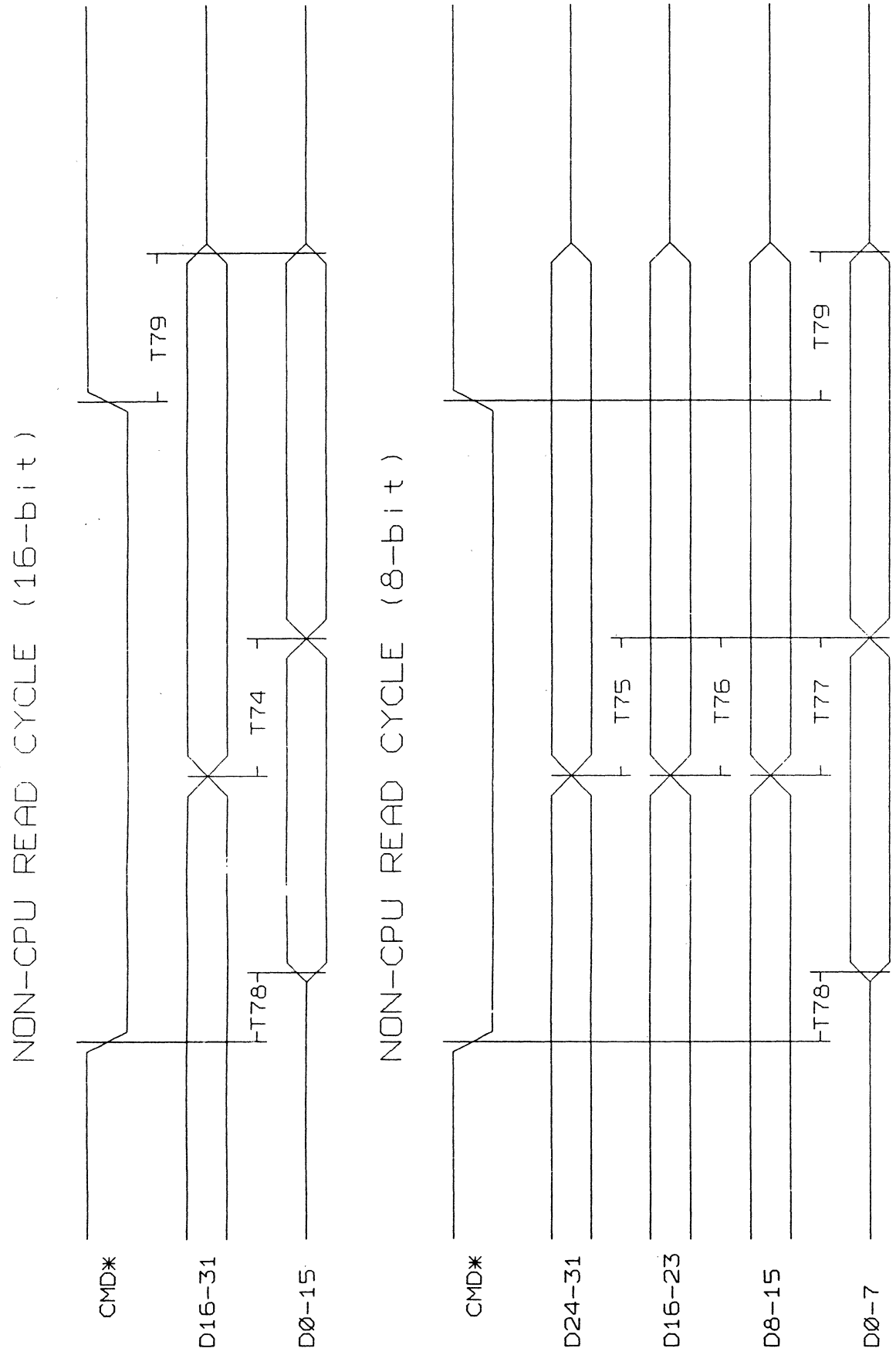
NON-CPU WRITE CYCLE (16-bit)



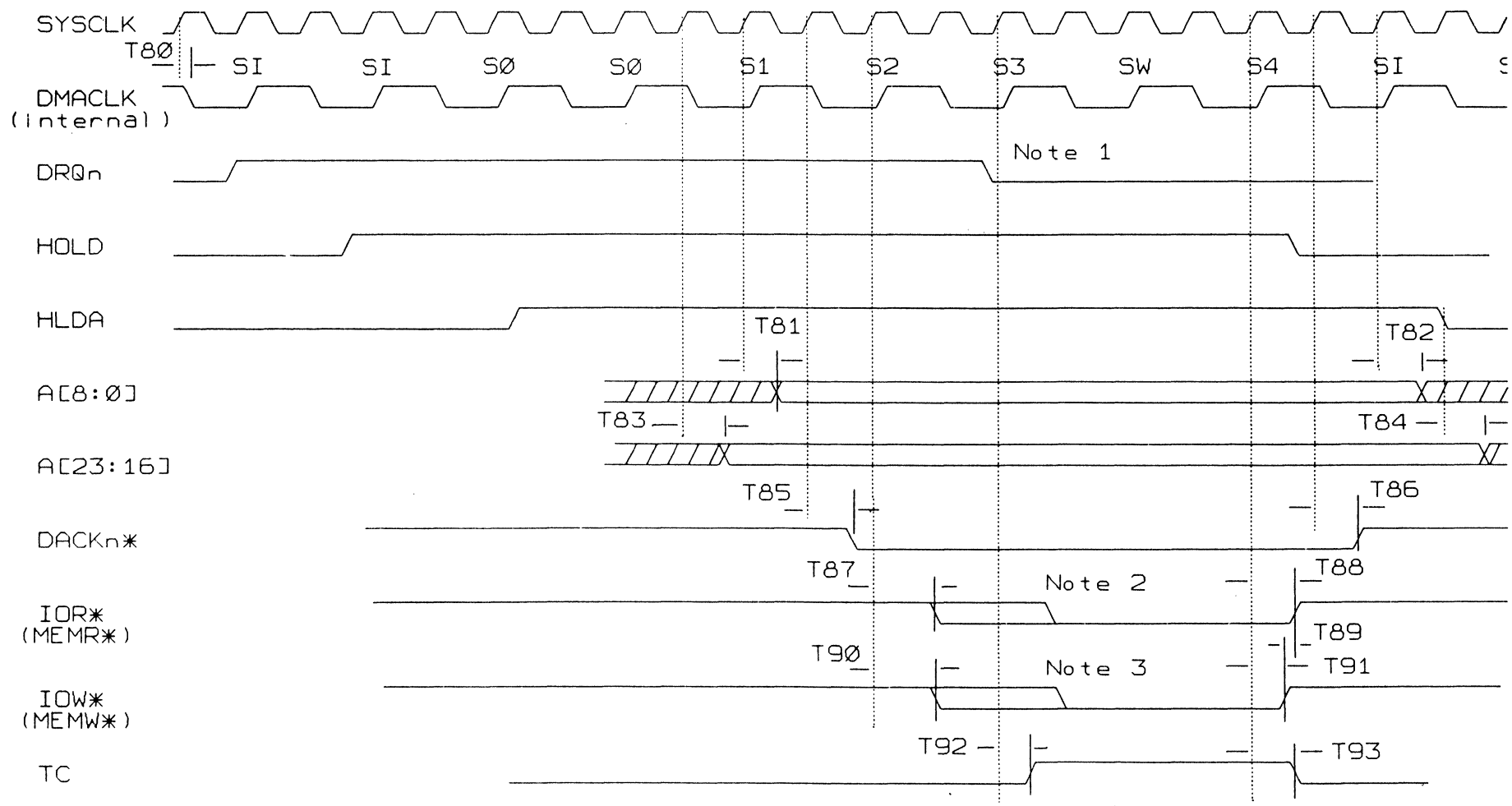
NON-CPU WRITE CYCLE (8-bit)



Timing Diagram



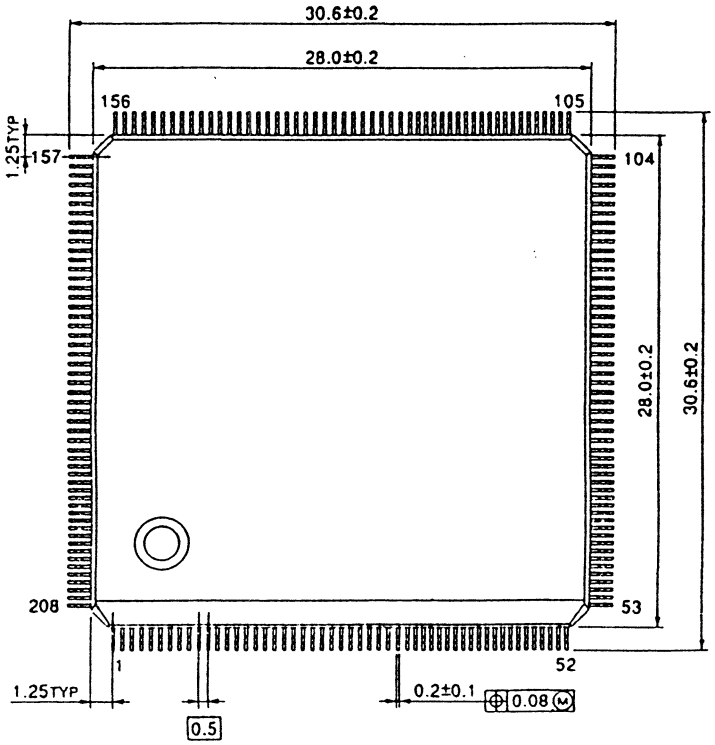
DMA TIMING

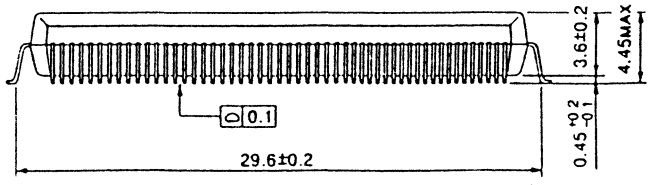


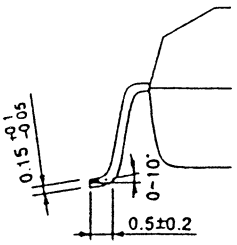
Note 1 : DREQ should be held active until DACK is asserted .
Note 2 : The first high to low transition is for normal read .
The second transition is for delay MEMRD# .
Note 3 : The first high to low transition is for extended write .
The second transition is for normal write .

MECHANICAL DIMENSION (FOR SiS85C460)

QFP208-P (208-Pin Plastic Flat Package) Unit: mm

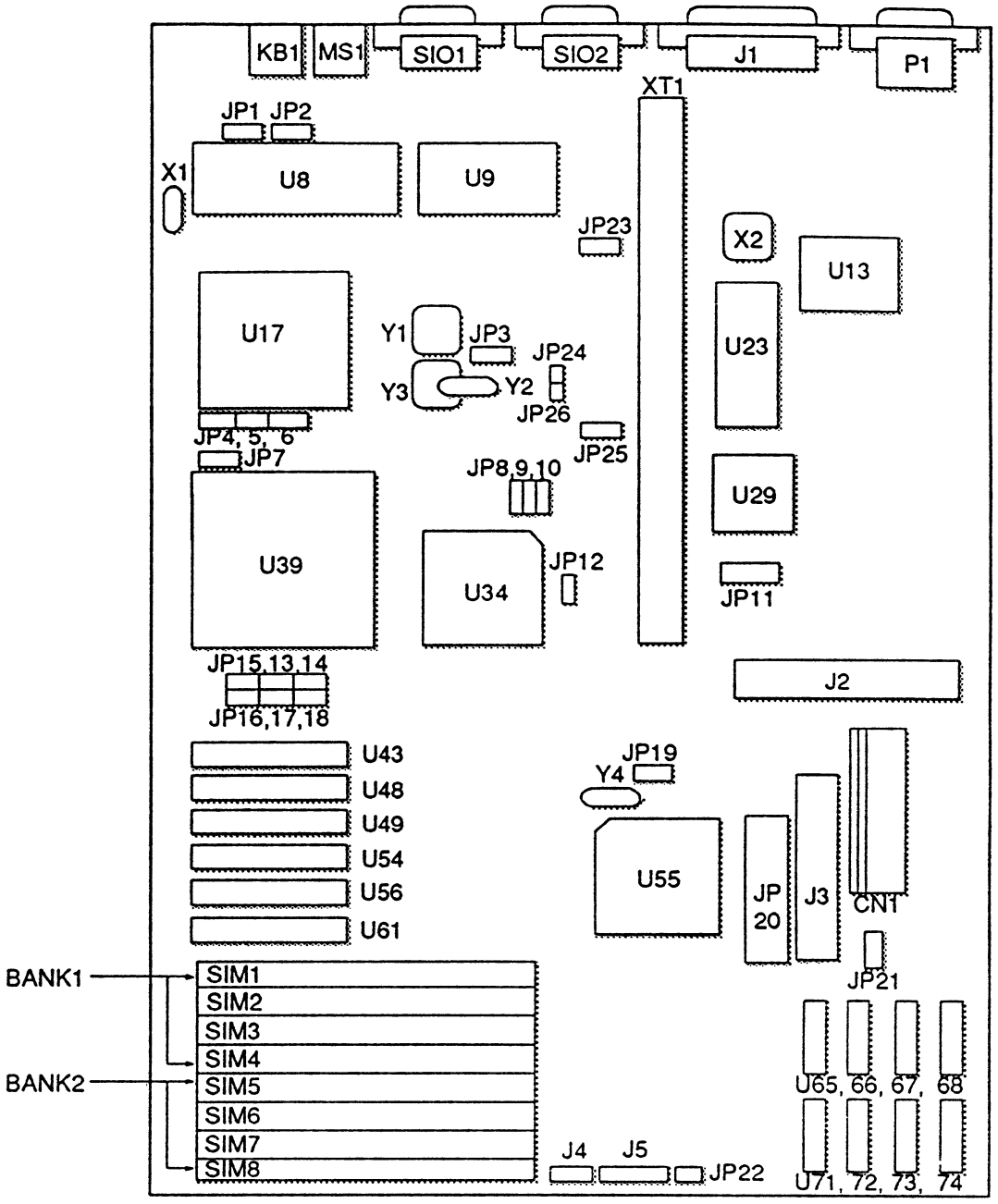






Chapter 4. System Board Jumper Settings

CPU related Jumper Settings
Cache Memory related Jumper Settings
Video related Jumper Settings
Interrupt related Jumper Settings
Connectors


KB1
MS1
SIO1
SIO2
J1
P1
XT1
JP1 JP2
X1
U8
U9
JP23
X2
U13
U17
Y1
JP3
JP24
U23
Y3
Y2
JP26
JP4, 5, 6
JP7
JP25
JP8,9,10
U29
U39
U34
JP12
JP11
JP15,13,14
J2
JP16,17,18
U43
U48
U49
U54
U56
U61
JP19
Y4
U55
JP 20
J3
CNT
JP21
BANK1
BANK2
SIM1
SIM2
SIM3
SIM4
SIM5
SIM6
SIM7
SIM8
U65, 66, 67, 68
J4
J5
JP22
U71, 72, 73, 74

This chapter describes that how to configure your system, when you need, using by system board jumpers. The following describes the location of the jumpers and connectors on the main board.

CPU related Jumper Settings

* CPU Select (JP4,JP5,JP7)

CPU	JP4	JP5	JP6	JP7
80486DX/DX2	1-2	Close	2-3	1-2
80487SX	1-2	Close	1-2	2-3
80486SX (PQFP)	2-3	Open	Open	2-3
80486SX (PGA)	2-3	Open	Open	1-2

* CPU Clock Speed Select (JP3,JP12)

CPU	JP3	JP12
80486DX-33	1-2	1-2
80486DX2-50	2-3	1-2
80486DX2-66	1-2	1-2
80486SX-25	2-3	1-2
80486SX-33	1-2	1-2

Cache Memory related Jumper Settings

* Cache Memory Configuration
  - Tag SRAM : 15ns
  - Dirty SRAM : 15ns
  - Data SRAM : 20ns

* Cache Data SRAM Select (JP15,JP16)

Cache Size (U49,54,56,61)	JP15	JP16
80486DX-33	2-3	2-3
80486DX2-50	1-2	1-2

* Cache Dirty SRAM Select (JP14,JP18)

Cache Size	U48	JP14	JP18
32KB	8Kb* x 8	2-3	2-3
128KB	32Kb x 8	1-2	1-2

Kb* : Kbit

* Cache Tag SRAM Select (JP13,JP17)

Cache Size	U43	JP13	JP17
32KB	8Kb x 8	2-3	2-3
128KB	32Kb x 8	1-2	1-2

Video related Jumper Settings

* Internal / External Video Select (JP21)

	JP21(1-2,3-4,5-6,7-8,9-10)	Remarks
Internal Video Use	All Close	Default
Internal Video Disable	All Open	—

* IRQ9 Enable / Disable (JP19)

IRQ9	JP19
Disable	Open
Enable	Close

Interrupt related Jumper Settings

	JP23	JP24	JP25	JP26
IRQ5, IRQ10	1-3 2-4	1-3 2-4	1-2 3-4	1-2 3-4
IRQ5, IRQ11	1-3 2-4	1-3 2-4	1-3 2-4	1-3 2-4
IRQ9, IRQ10	1-2 3-4	1-2 3-4	1-2 3-4	1-2 3-4
IRQ9, IRQ11	1-2 3-4	1-2 3-4	1-3 2-4	1-3 2-4

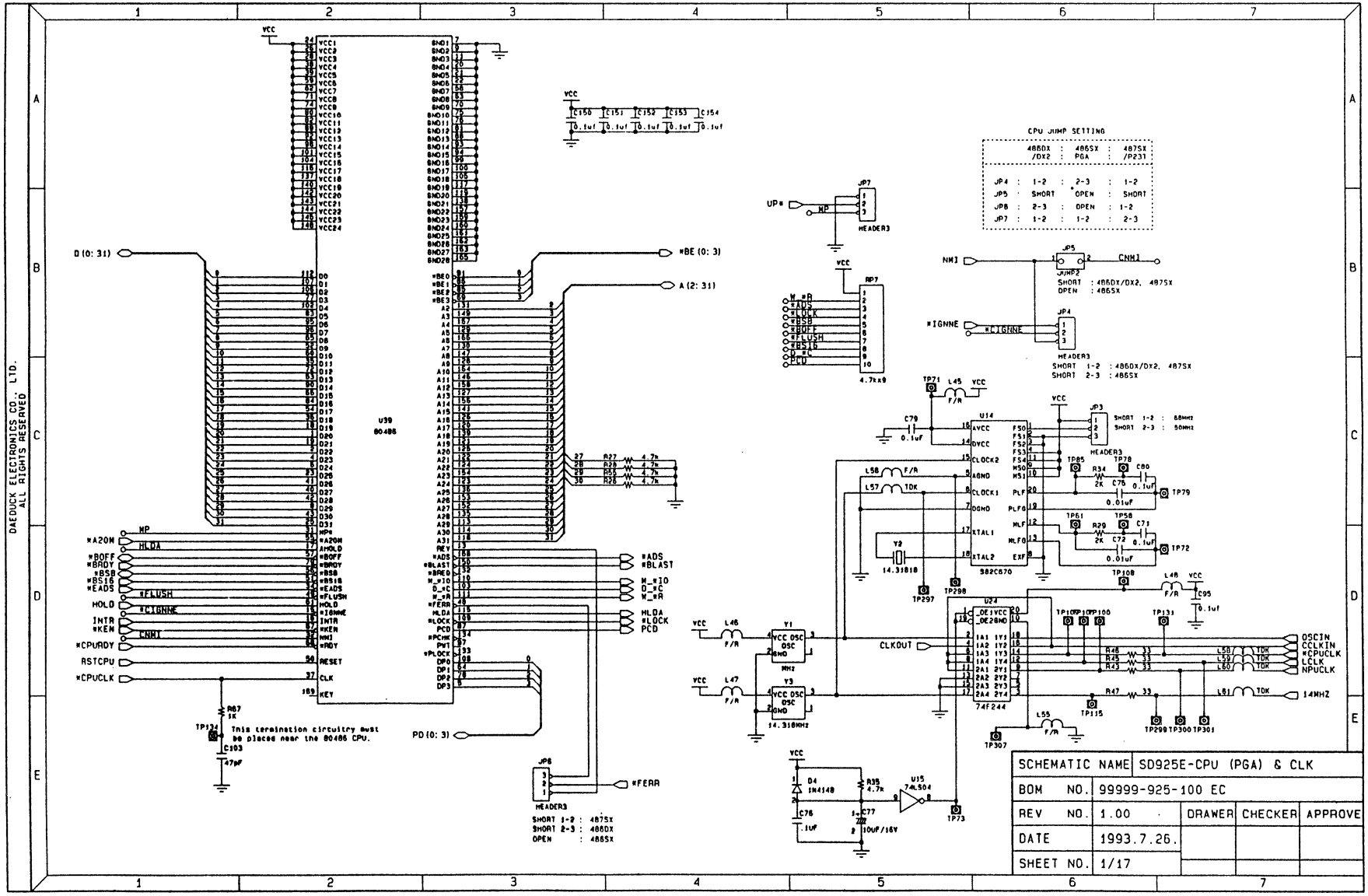
For a certain expansion card, its interrupt signal width is very short. Thus interrupts form these cards may not be recognized correctly by the system.
Jumpers JP23, 24, 25, 26 are provided to select interrupt lines that can process those short interrupt signals. You can use only two signals at the same time for this purpose. From factory IRQ9 and IRQ11 are selected.

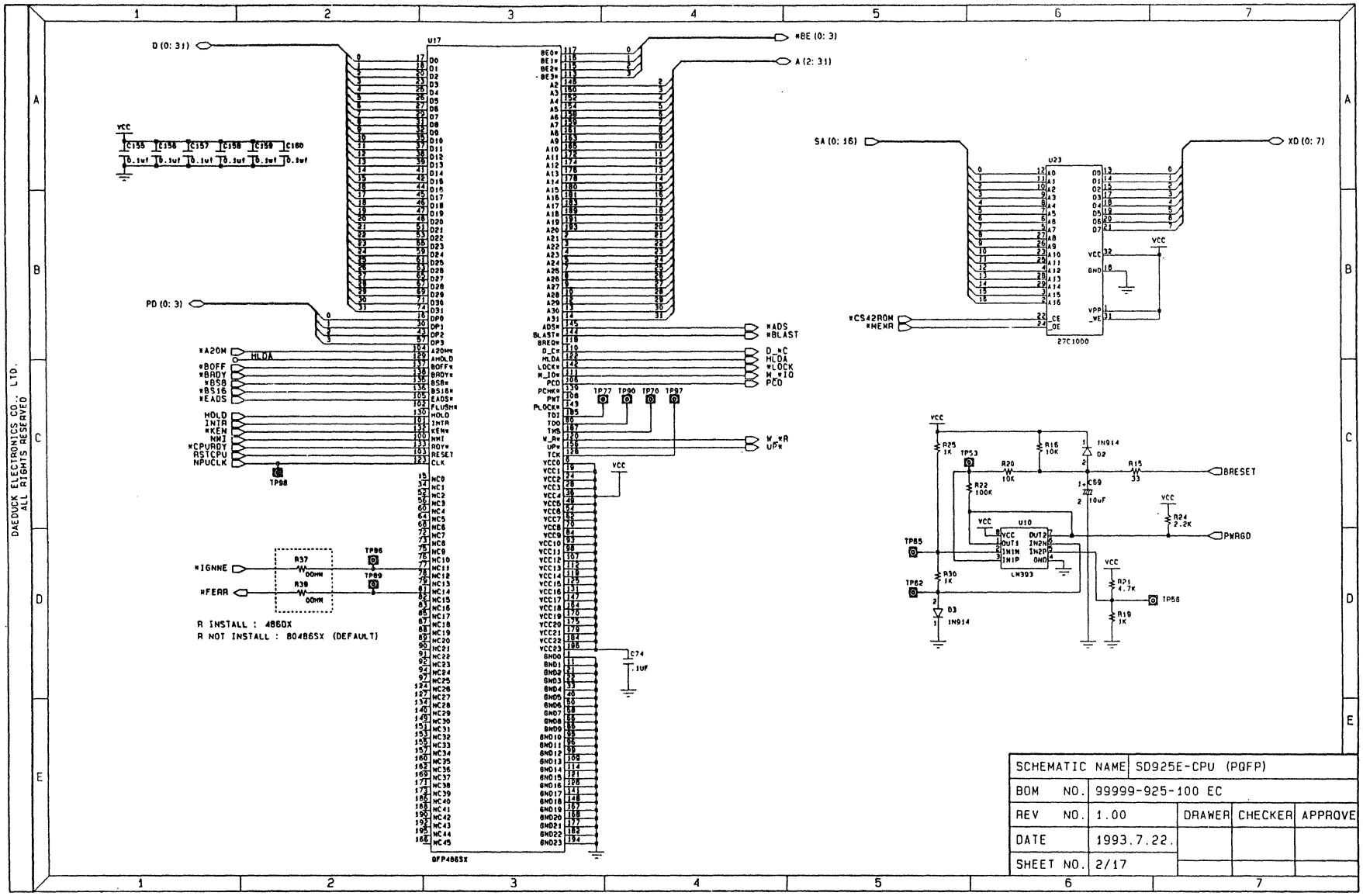
Connectors

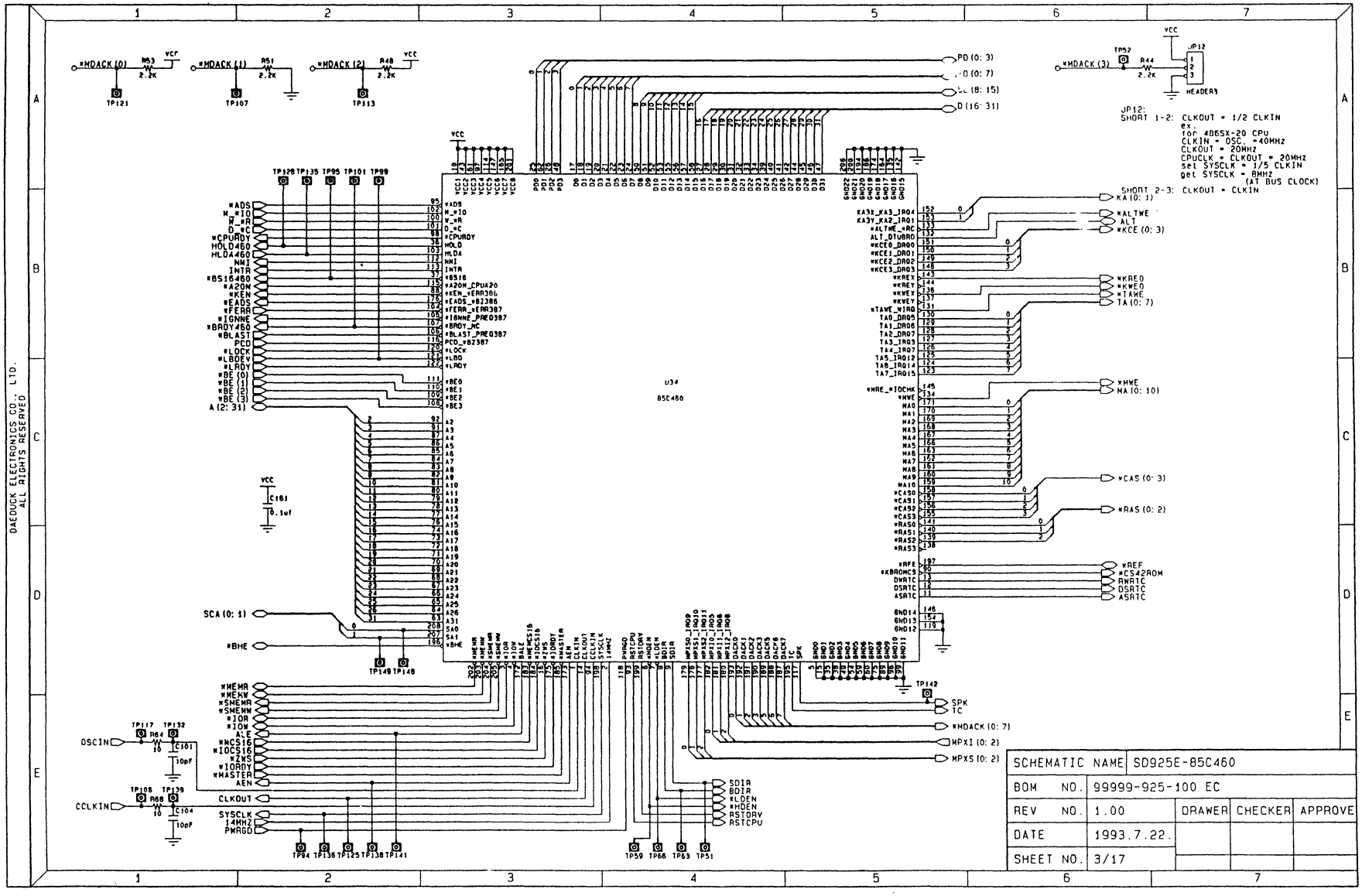
Description	Connector
Printer Port(= Parallel Port)	J1
Serial Port	SI)!, SI02
Keyboard Port	KB1
Mouse Port	MS1
Turbo LED, Kdy-Lock, Reset, Power LED Connectoe	J5
Speaker Connector	JP22
Power Connector	CN1
IDE HDD Connector	J2
FDD Connector	J3
IDE HDD Active-LED Connector	J4

Chapter 5. Schematics

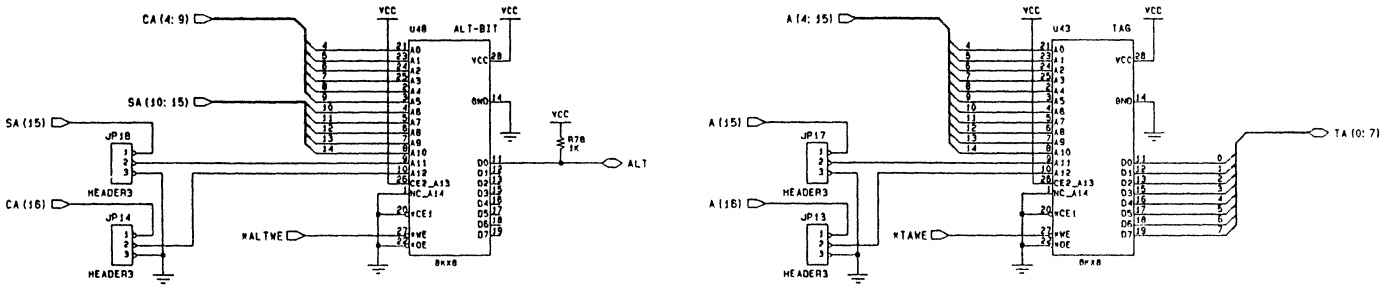
Main Board Schematic
Main Board Component Layout
Main Board PCB Pattern
Power Supply Schematic
Power Supply Component Layout
Bus Board Schematic
Bus Board Component Layout
Bus Board PCB Patten


DAEDUCK ELECTRONICS CO., LTD.
ALL RIGHTS RESERVED
CPU JUMP SETTING
486DX /DX2 : 486SX PGA : 487SX /P231
JP4 : 1-2 : 2-3 : 1-2
JP5 : SHORT : OPEN : SHORT
JP6 : 2-3 : OPEN : 1-2
JP7 : 1-2 : 1-2 : 2-3
D(0:31)
*BE(0:3)
A(2:31)
PD(0:3)
U39
80486
U14
82C670
U24
74F244
Y1
14.318MHz
Y2
14.31818
Y3
14.318MHz
CLKOUT
OSCIN
CCLKIN
*CPUCLK
LCLK
NPUCLK
14MHZ
This termination circuitry must be placed near the 80486 CPU.
SCHEMATIC NAME SD925E-CPU (PGA) & CLK
BOM NO. 99999-925-100 EC
REV NO. 1.00
DATE 1993.7.26.
SHEET NO. 1/17
DRAWER
CHECKER
APPROVE


DAEDUCK ELECTRONICS CO., LTD.
ALL RIGHTS RESERVED
D (0: 31)
PD (0: 3)
U17
*BE (0: 3)
A (2: 31)
*ADS
*BLAST
D_*C
HLDA
*LOCK
M_*IO
PCD
W_*R
U*R
*A20M
HLDA
*BOFF
*BRDY
*BS8
*BS16
*EADS
HOLD
INTR
*KEN
NMI
*CPURDY
RSTCPU
NPUCLK
TP98
TP77
TP90
TP70
TP87
*IGNNE
*FERR
R37
R38
00HM
TP86
TP89
R INSTALL : 486DX
R NOT INSTALL : 80486SX (DEFAULT)
PPP486SX
SA (0: 16)
XD (0: 7)
U23
27C1000
*CS42ROM
*MEMR
VCC
GND
VPP
_WE
_OE
BRESET
PWRGD
U10
LM393
TP85
TP82
TP58
R25 1K
R16 10K
R20 10K
R15 33
R22 100K
R24 2.2K
R30 1K
R21 4.7K
R19 1K
C59 10uF
C74 .1uF
D2 1N914
D3 1N914
TP53
SCHEMATIC NAME SD925E-CPU (PQFP)
BOM NO. 99999-925-100 EC
REV NO. 1.00
DATE 1993.7.22.
SHEET NO. 2/17
DRAWER
CHECKER
APPROVE


DAEDUCK ELECTRONICS CO., LTD.
ALL RIGHTS RESERVED
SCHEMATIC NAME SD925E-85C460
BOM NO. 99999-925-100 EC
REV NO. 1.00
DATE 1993.7.22.
SHEET NO. 3/17
DRAWER
CHECKER
APPROVE
JP12:
SHORT 1-2: CLKOUT = 1/2 CLKIN
ex.
for 486SX-20 CPU
CLKIN = OSC =40MHZ
CLKOUT = 20MHZ
CPUCLK = CLKOUT = 20MHZ
set SYSCLK = 1/5 CLKIN
get SYSCLK = 8MHZ
(AT BUS CLOCK)
SHORT 2-3: CLKOUT = CLKIN
U34
85C460
HEADER3

CACHE SYSTEM



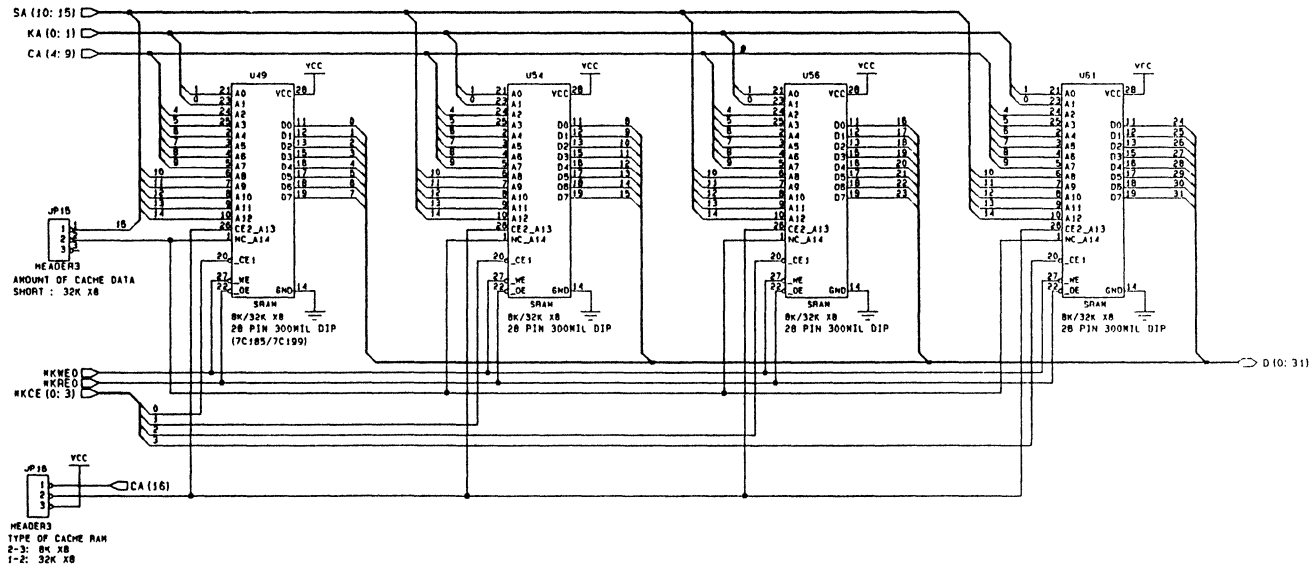
Cache Size	TAG		ALT	
	JP13	JP17	JP14	JP18
32K	2-3	2-3	2-3	2-3
128K	1-2	1-2	1-2	1-2

DAEDUCK ELECTRONICS CO., LTD.
ALL RIGHTS RESERVED

SCHEMATIC NAME	SD925E-CACHE TAG & DIRTY BIT			
BOM NO.	99999-925-100 EC			
REV NO.	1.00	DRAWER	CHECKER	APPROVE
DATE	1993.7.22.			
SHEET NO.	4/17			

DAEDUCK ELECTRONICS CO., LTD.
ALL RIGHTS RESERVED

CACHE SYSTEM

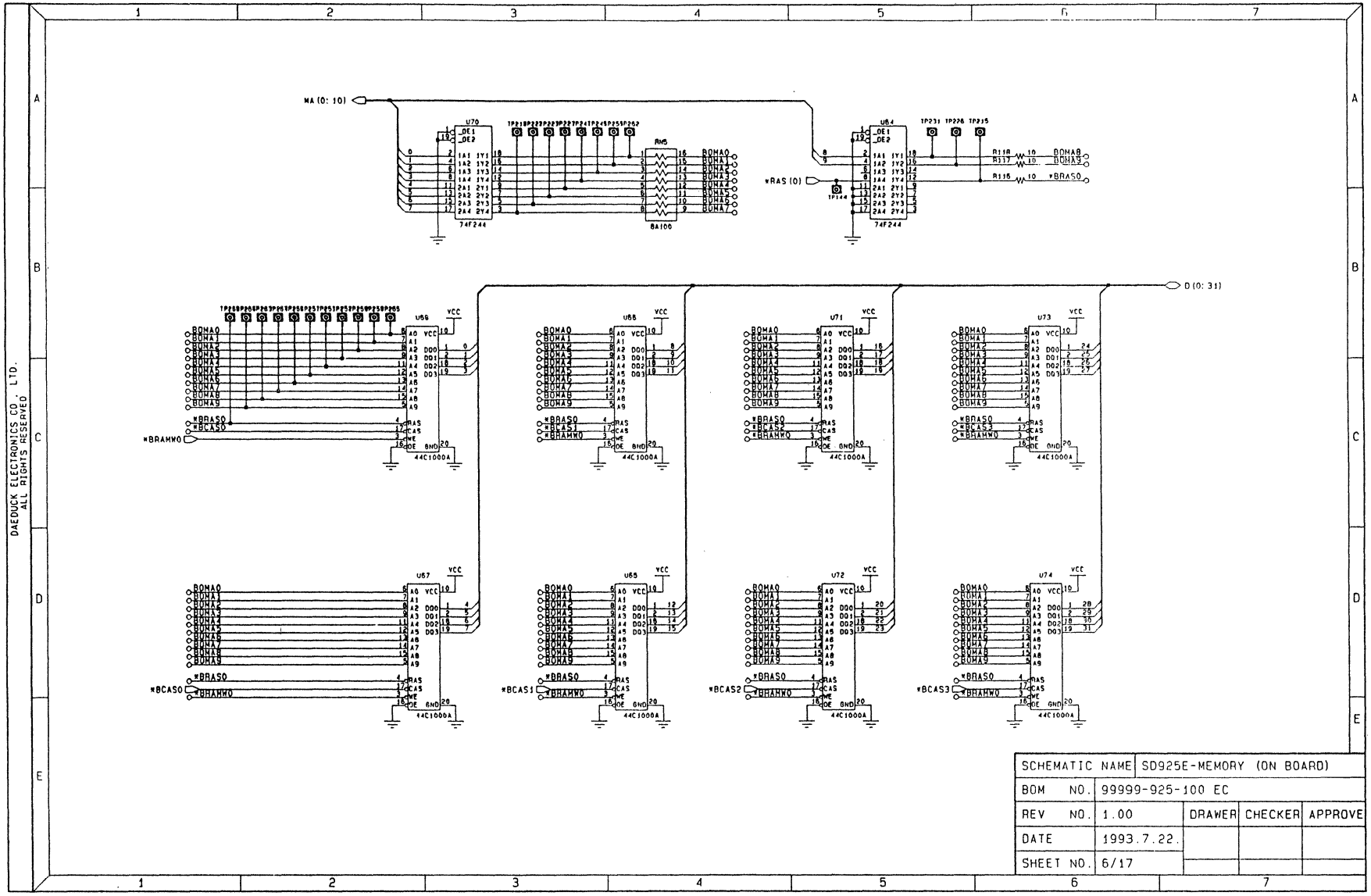


CACHE JUMPER SET

CACHE SIZE	DRAM TYPE	JP15	JP16
32KB	8K X 8	2-3	2-3
128KB	32K X8	1-2	1-2

SCHEMATIC NAME	SD925E-CACHE DATA MEMORY			
BOM NO.	99999-925-100 EC			
REV NO.	1.00	DRAWER	CHECKER	APPROVE
DATE	1993.7.22.			
SHEET NO.	5/17			

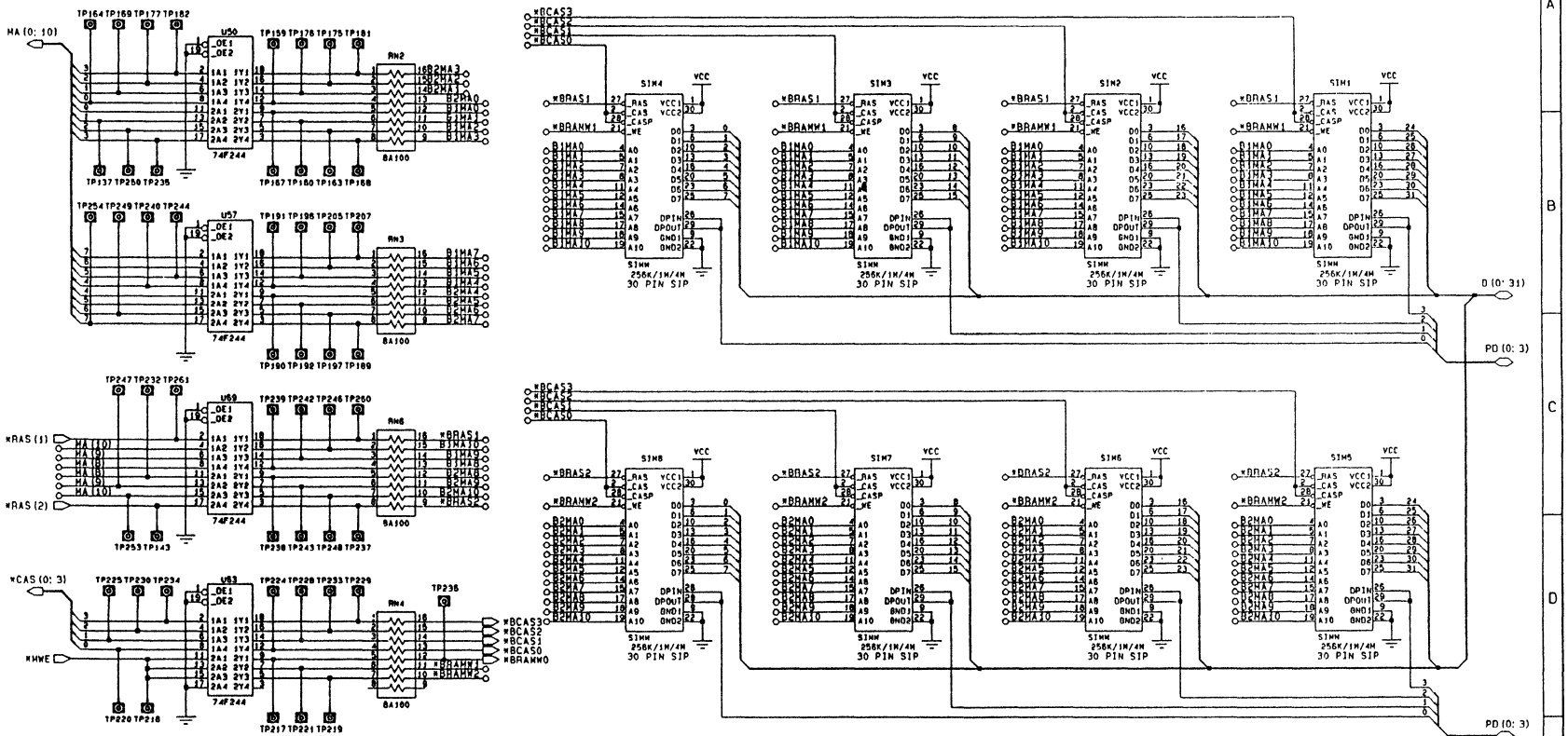
DAEDUCK ELECTRONICS CO., LTD.
ALL RIGHTS RESERVED



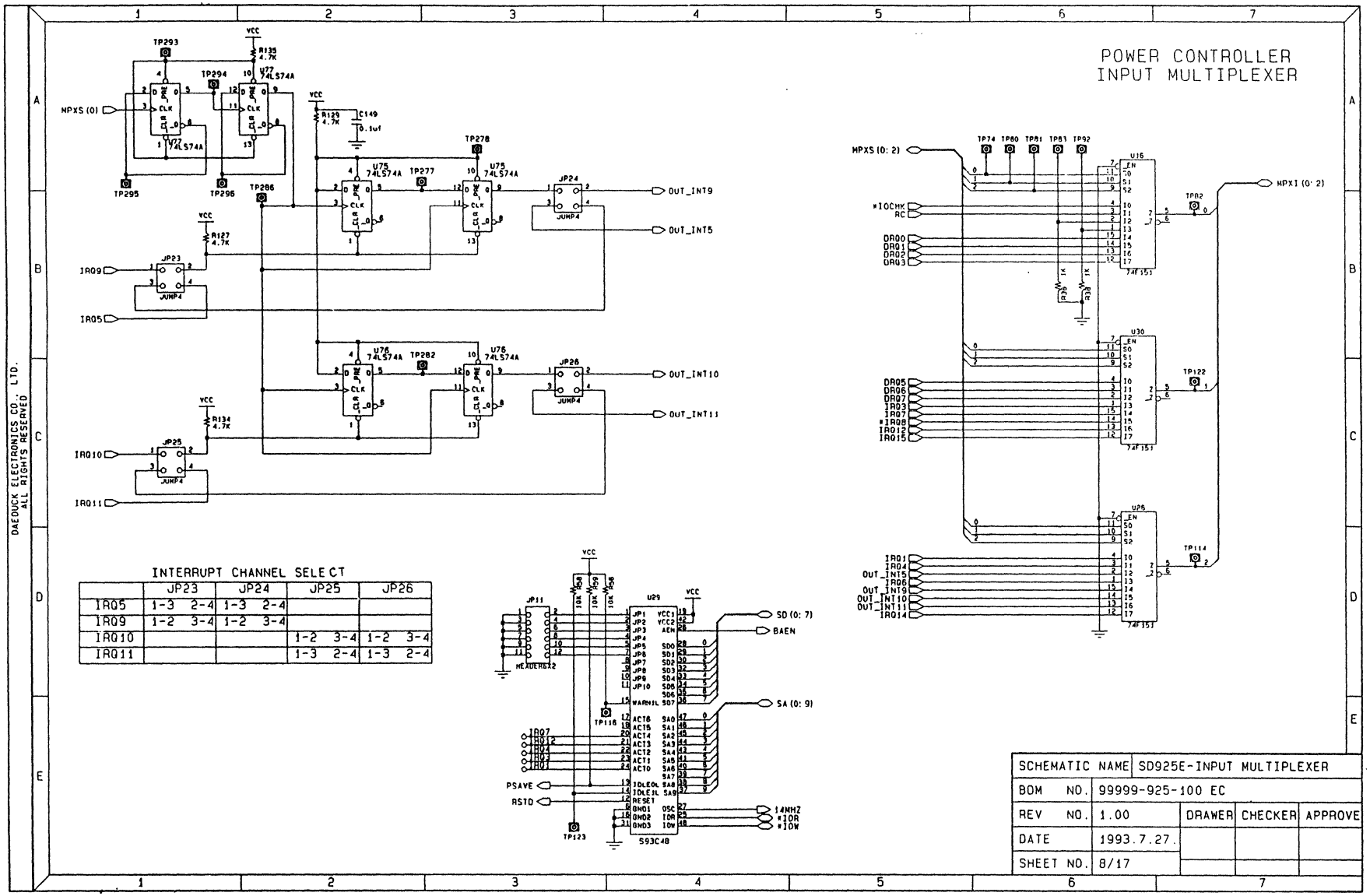
SCHEMATIC NAME	SD925E-MEMORY (ON BOARD)			
BOM NO.	99999-925-100 EC			
REV NO.	1.00	DRAWER	CHECKER	APPROVE
DATE	1993.7.22.			
SHEET NO.	6/17			

DAEDUCK ELECTRONICS CO., LTD.
ALL RIGHTS RESERVED

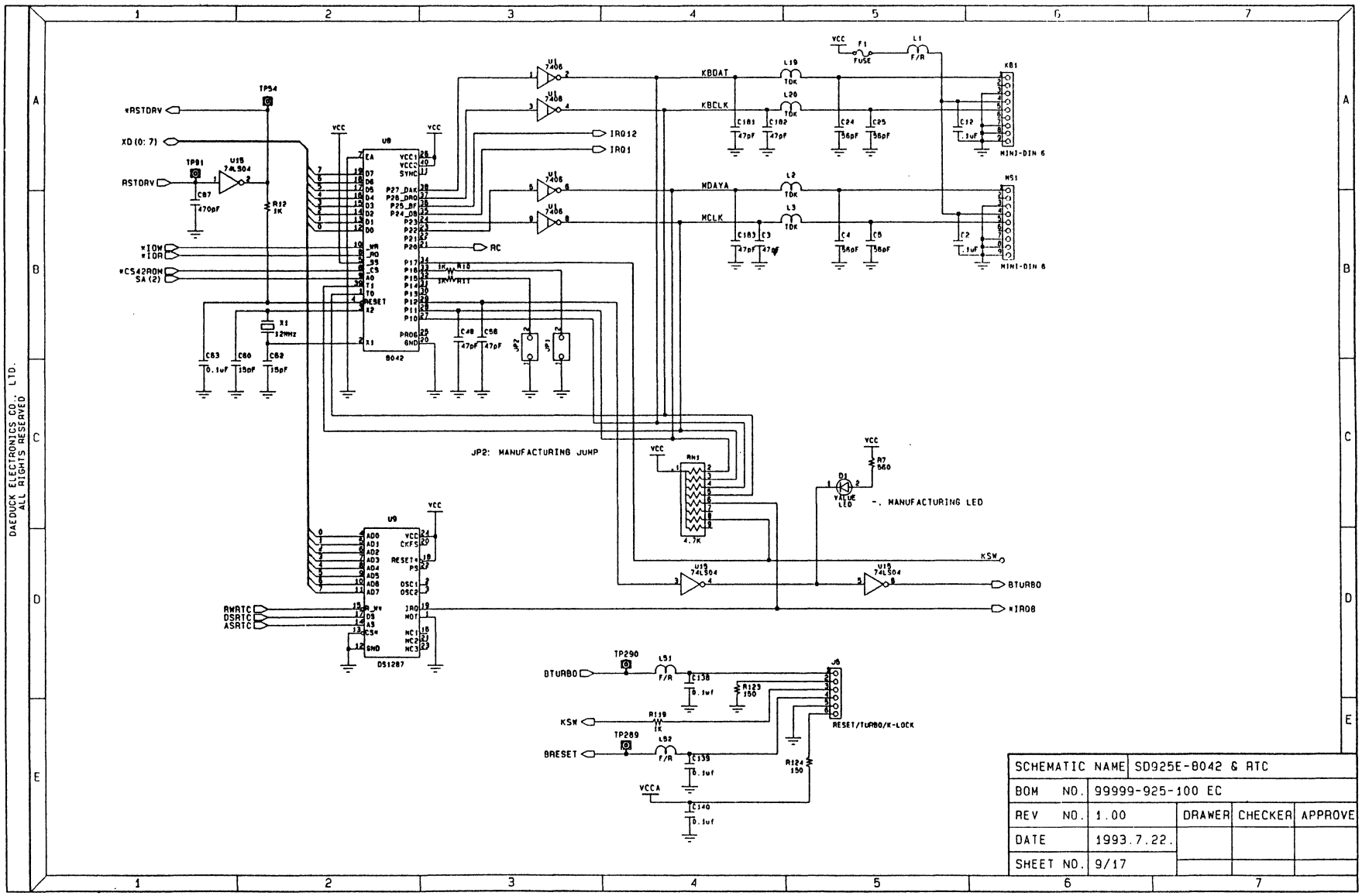
32MB DRAM SYSTEM



SCHEMATIC NAME	SD925E-MEMORY (EXTEND)			
BOM NO.	99999-925-100 EC			
REV NO.	1.00	DRAWER	CHECKER	APPROVE
DATE	1993.7.22.			
SHEET NO.	7/17			

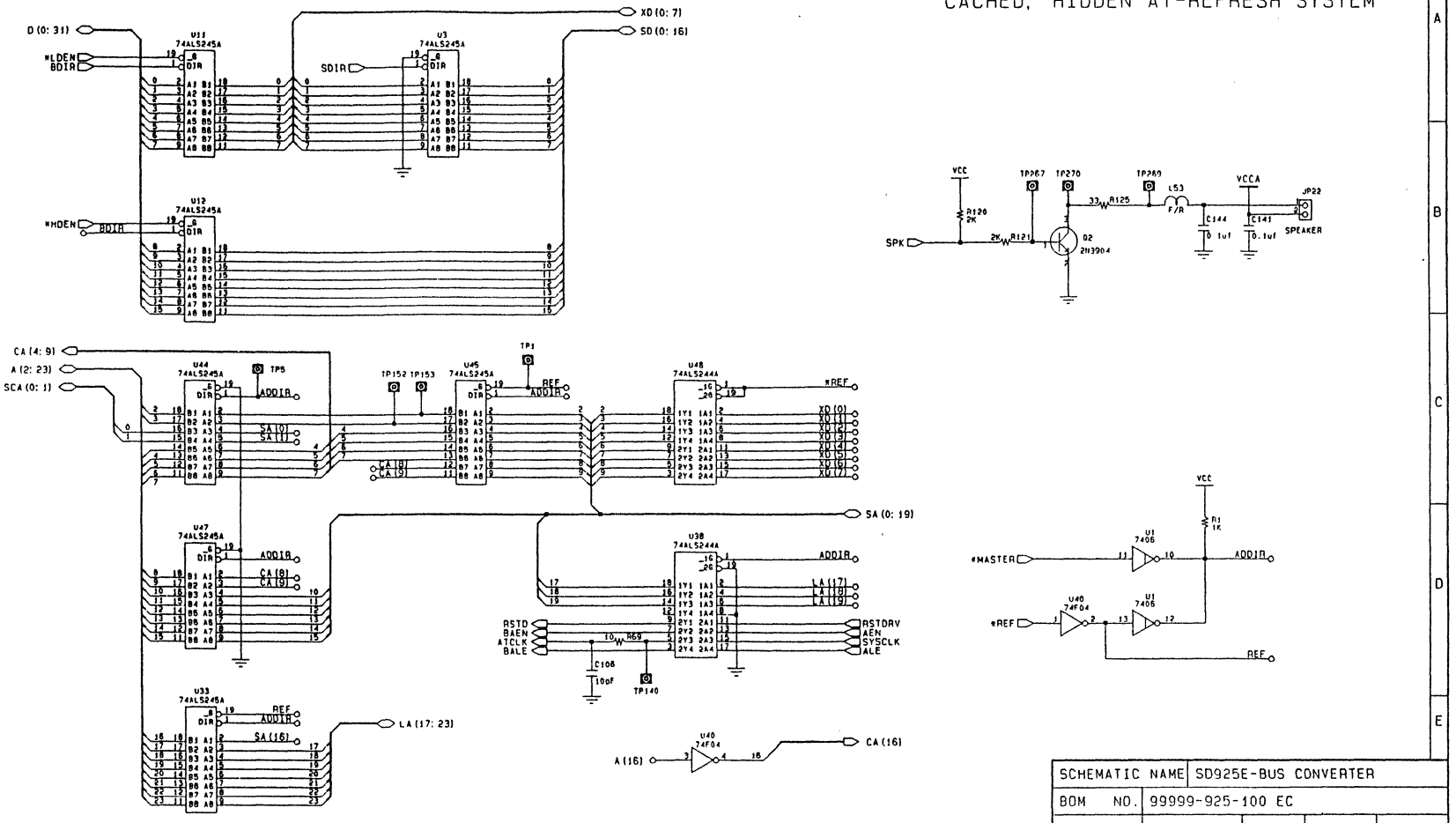


	JP23	JP24	JP25	JP26
IRQ5	1-3 2-4	1-3 2-4		
IRQ9	1-2 3-4	1-2 3-4		
IRQ10			1-2 3-4	1-2 3-4
IRQ11			1-3 2-4	1-3 2-4

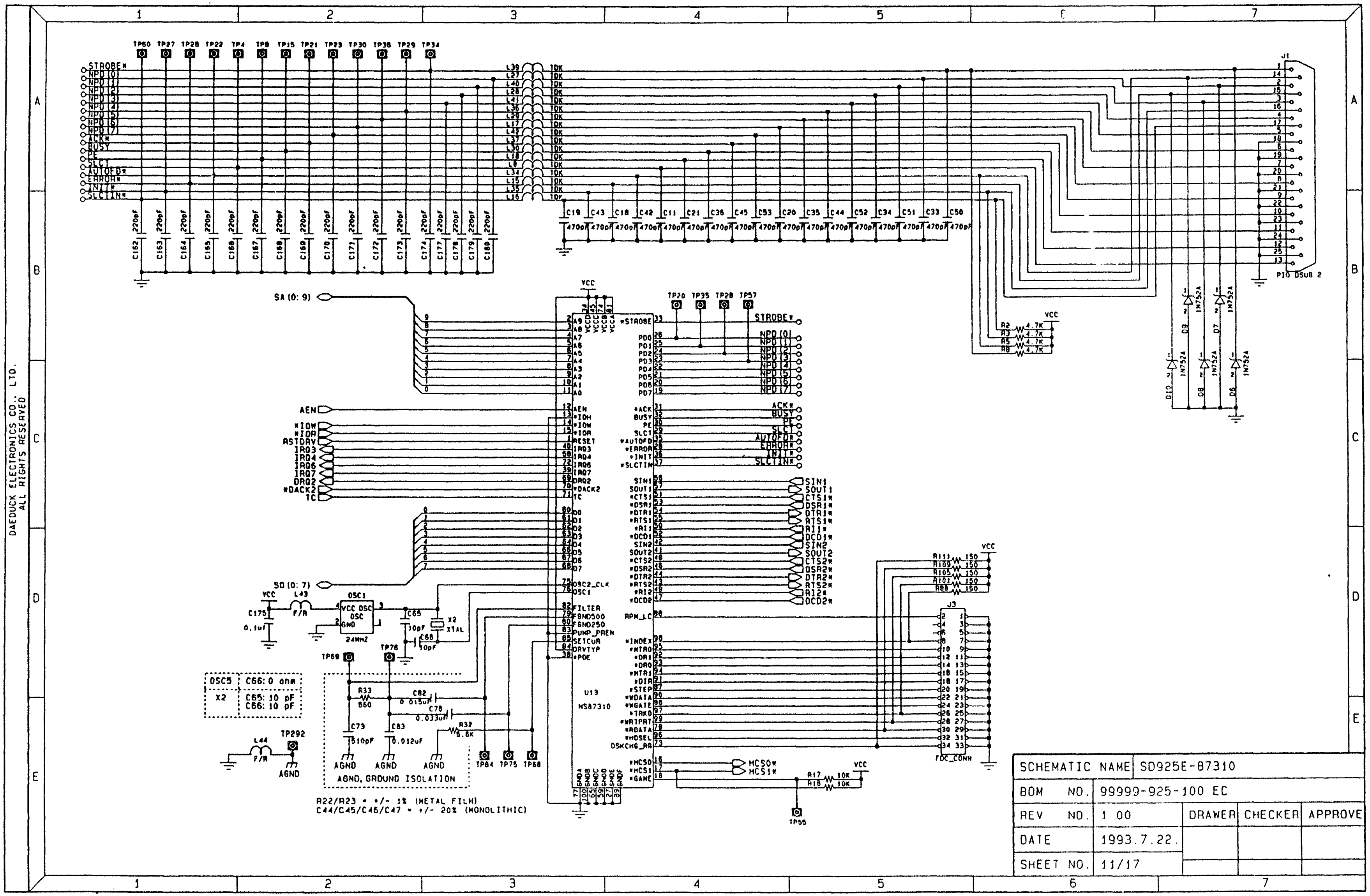

DAEDUCK ELECTRONICS CO., LTD.
ALL RIGHTS RESERVED
JP2: MANUFACTURING JUMP
-. MANUFACTURING LED
RESET/TURBO/K-LOCK
SCHEMATIC NAME SD925E-8042 & RTC
BOM NO. 99999-925-100 EC
REV NO. 1.00
DATE 1993.7.22.
SHEET NO. 9/17
DRAWER
CHECKER
APPROVE

DAEDUCK ELECTRONICS CO., LTD.
ALL RIGHTS RESERVED

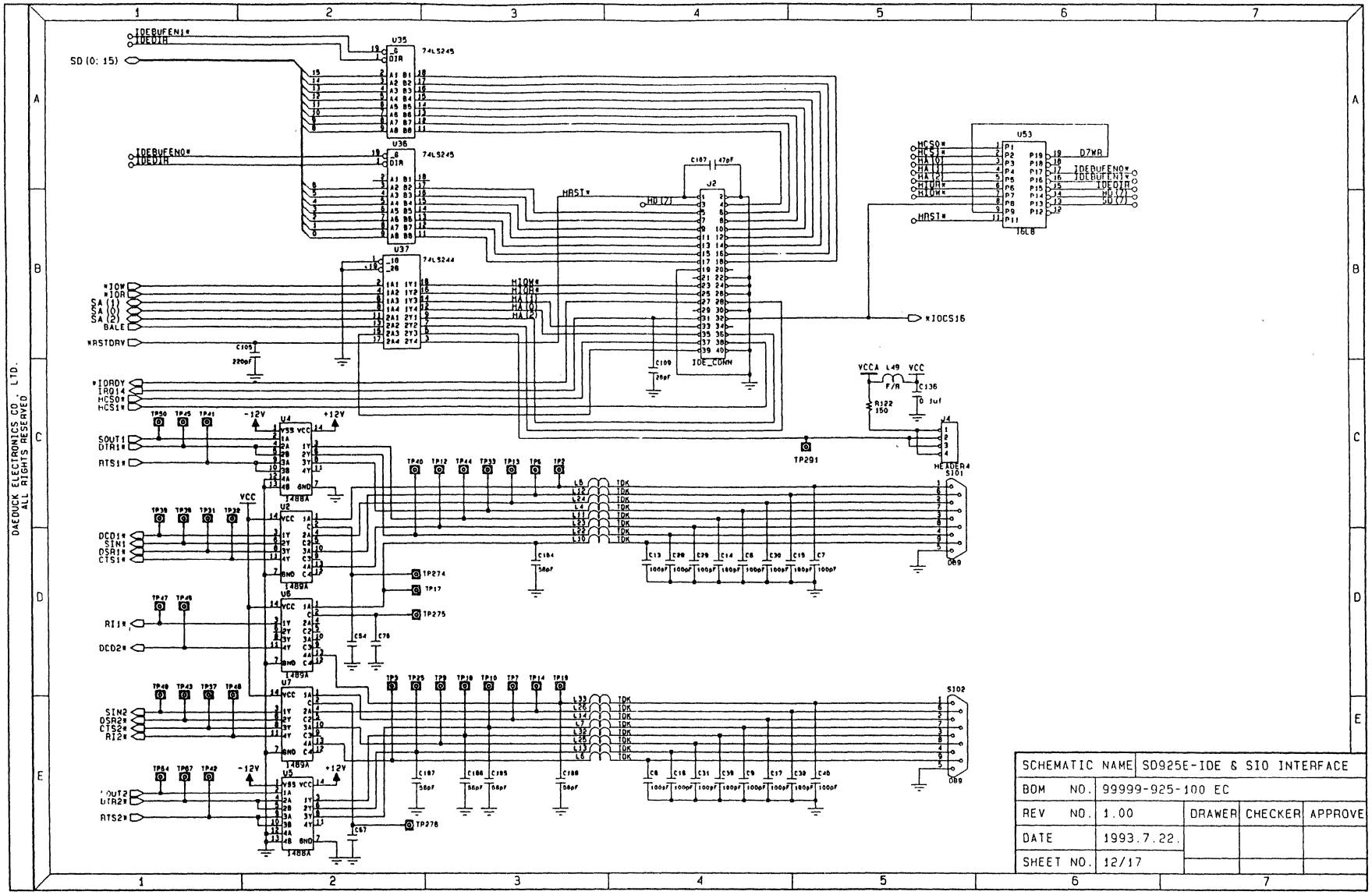
CACHED, HIDDEN AT-REFRESH SYSTEM

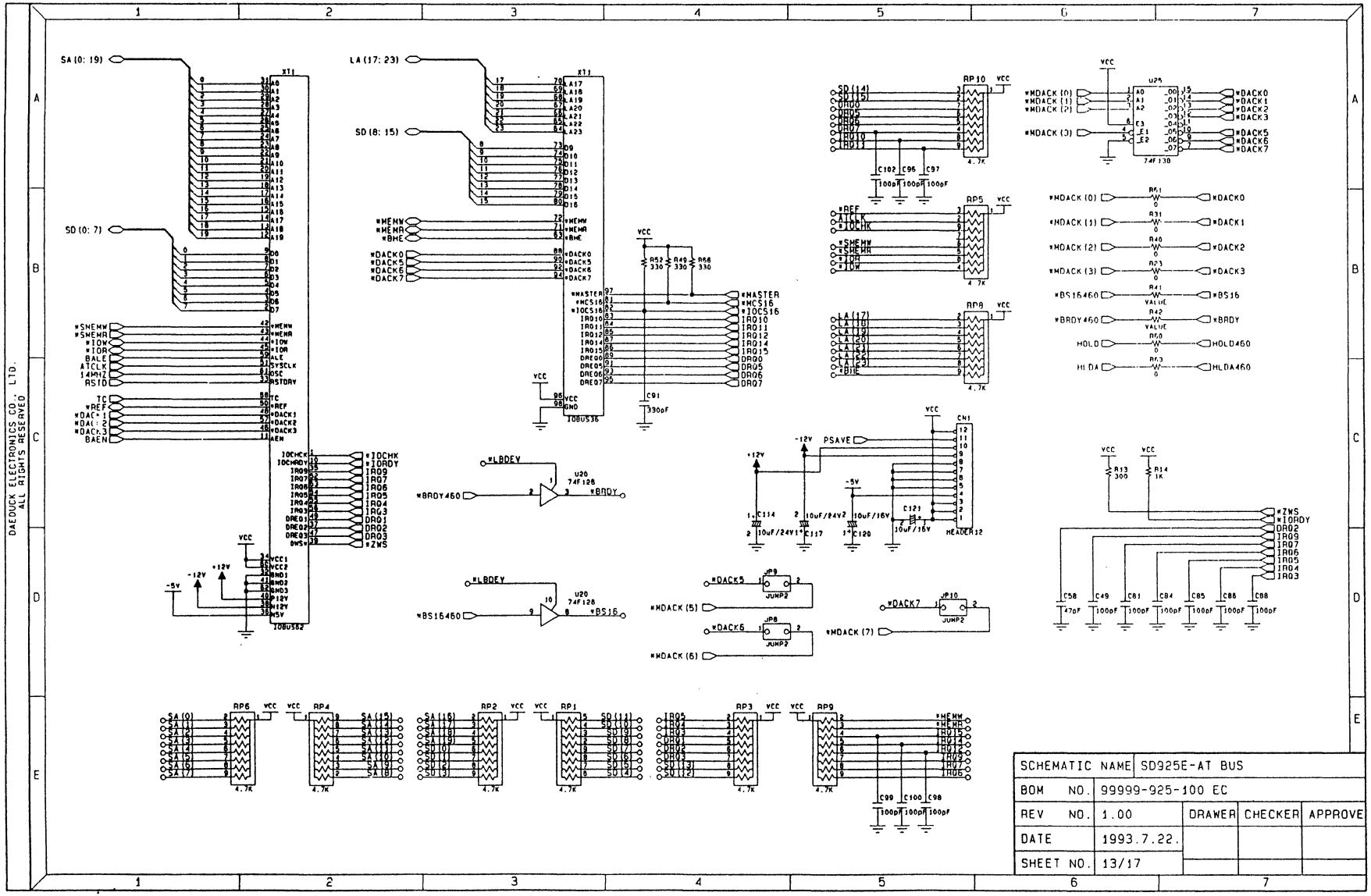


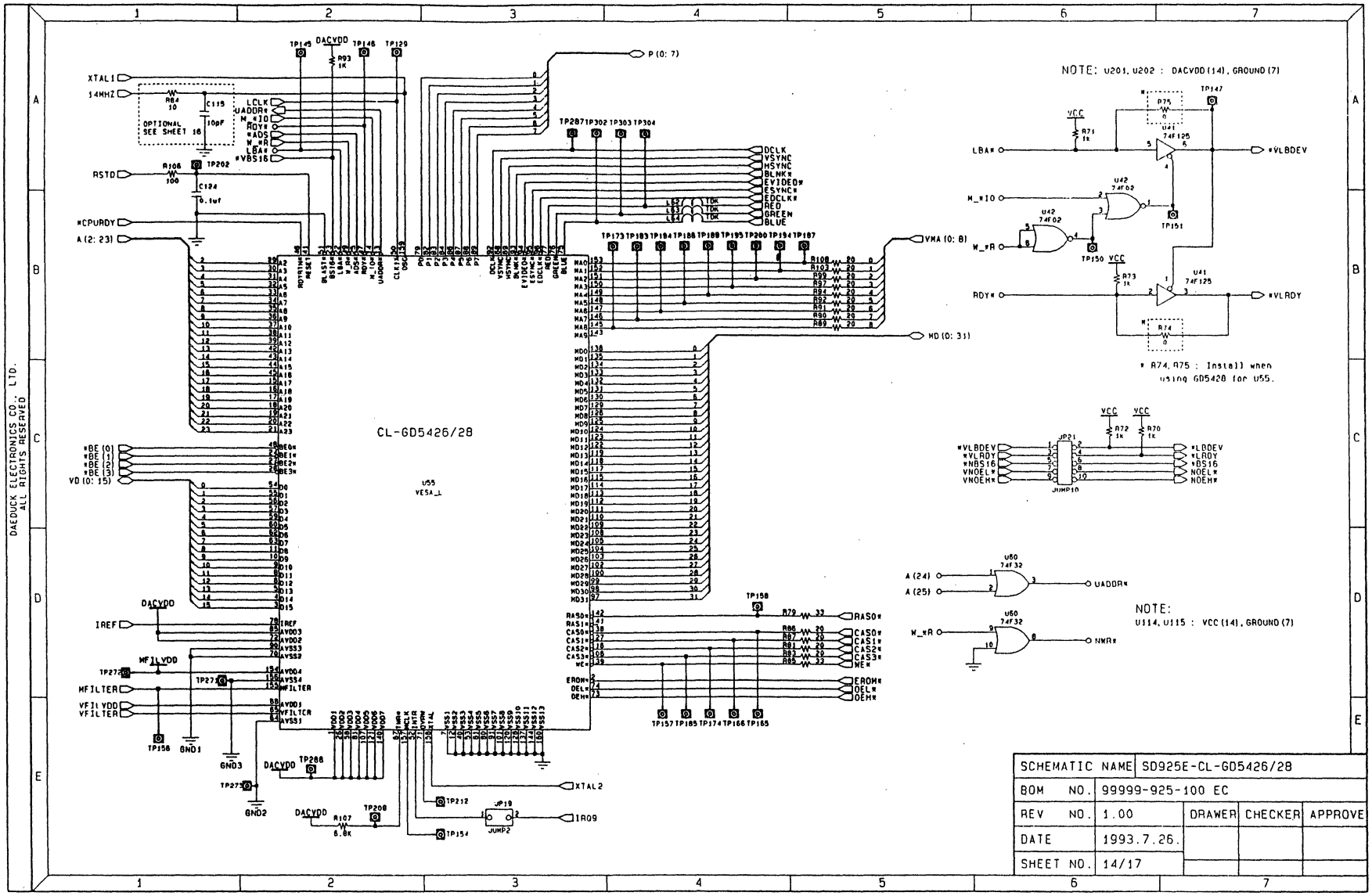
SCHEMATIC NAME	SD925E-BUS CONVERTER			
BOM NO.	99999-925-100 EC			
REV NO.	1.00	DRAWER	CHECKER	APPROVE
DATE	1993.7.22.			
SHEET NO.	10/17			



DAEDUCK ELECTRONICS CO., LTD.
ALL RIGHTS RESERVED
U13
NS87310
AGND, GROUND ISOLATION
R22/R23 = +/- 1% (METAL FILM)
C44/C45/C46/C47 = +/- 20% (MONOLITHIC)
PIO DSUB 2
FDC_CONN
SCHEMATIC NAME SD925E-87310
BOM NO. 99999-925-100 EC
REV NO. 1 00
DRAWER
CHECKER
APPROVE
DATE 1993.7.22.
SHEET NO. 11/17

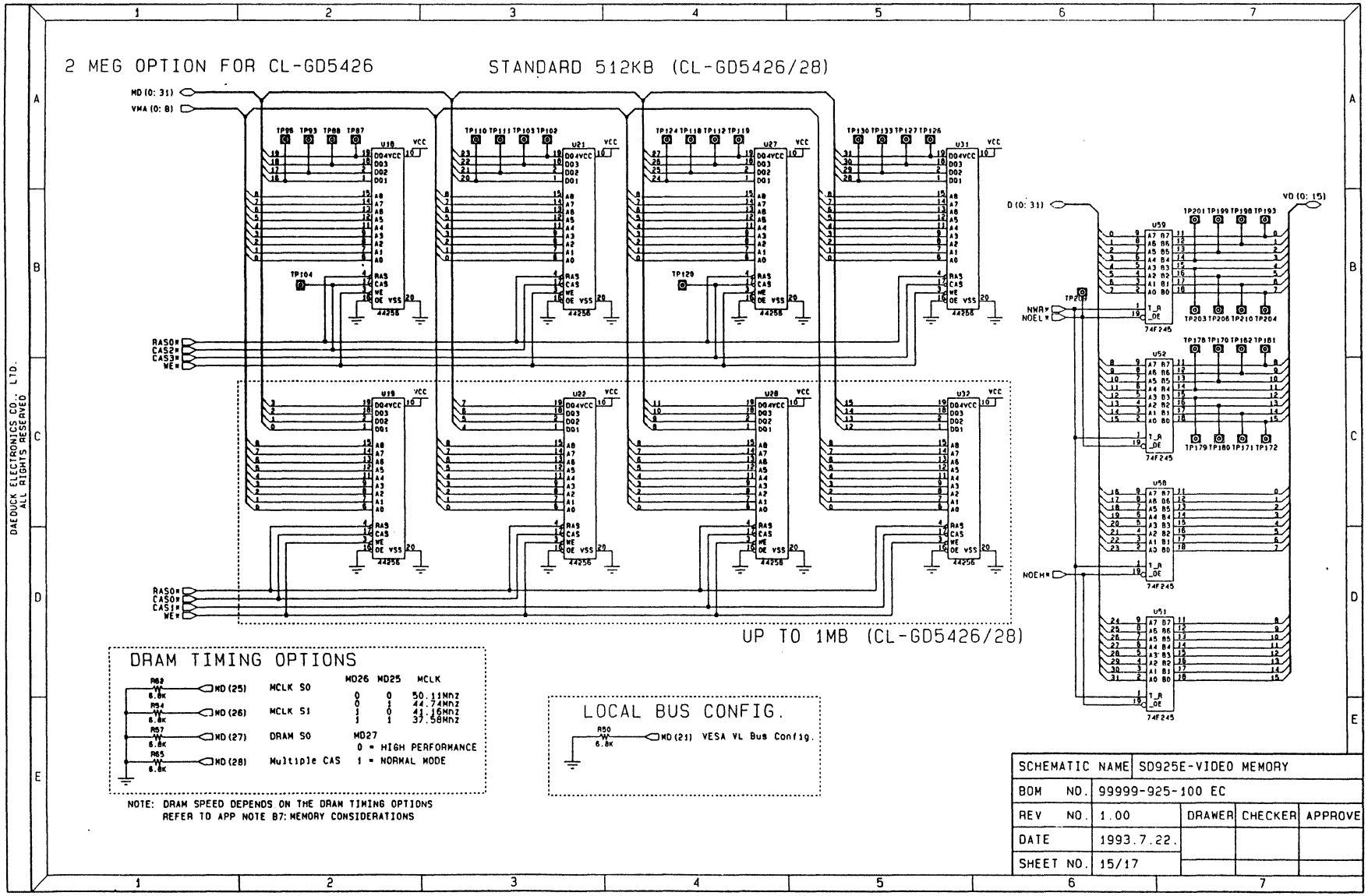

DAEDUCK ELECTRONICS CO., LTD.
ALL RIGHTS RESERVED
SCHEMATIC NAME SD925E-IDE & SIO INTERFACE
BOM NO. 99999-925-100 EC
REV NO. 1.00
DATE 1993.7.22.
SHEET NO. 12/17
DRAWER
CHECKER
APPROVE

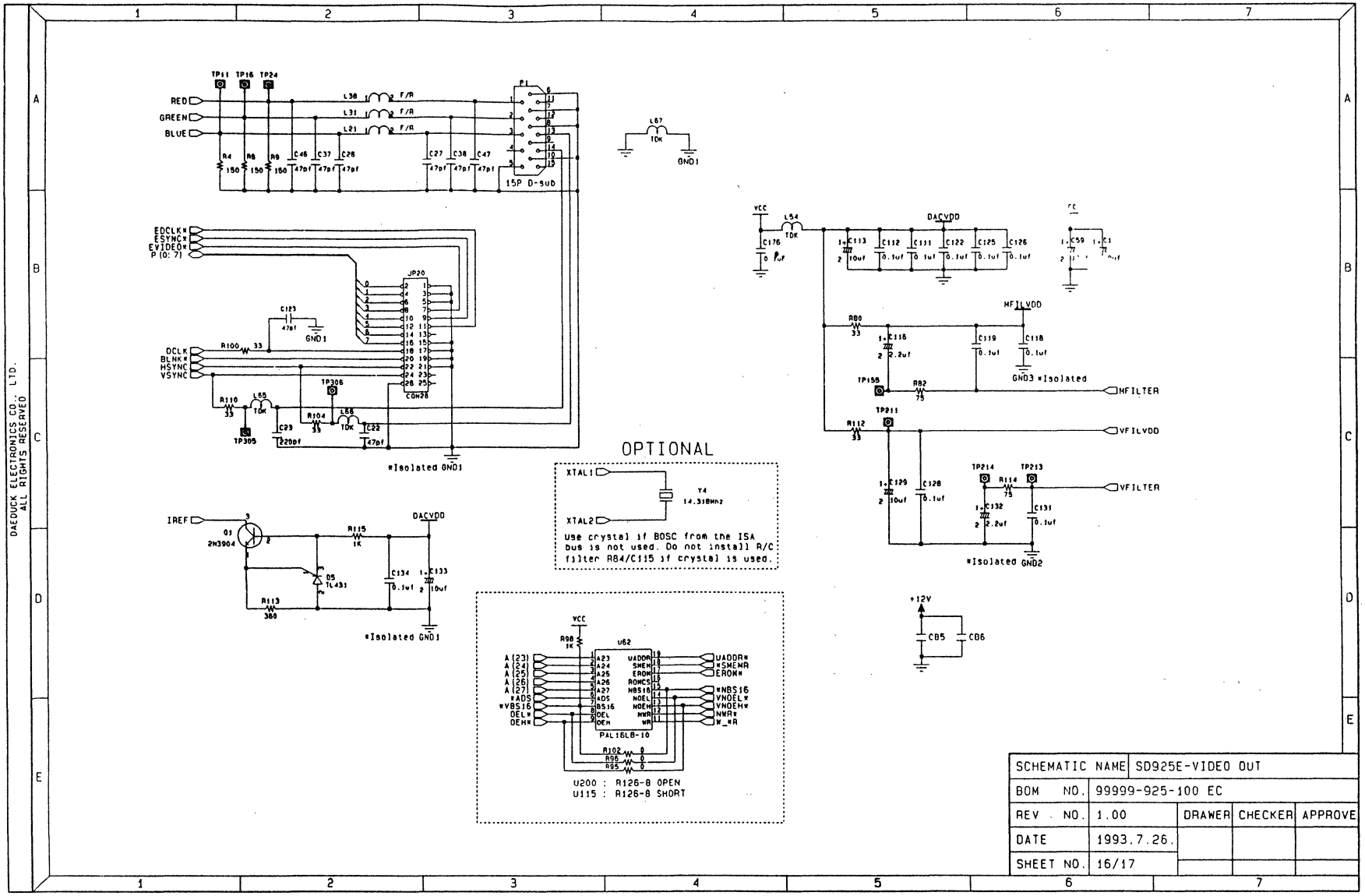

DAEDUCK ELECTRONICS CO., LTD.
ALL RIGHTS RESERVED
SA (0: 19)
SD (0: 7)
LA (17: 23)
SD (8: 15)
SD925E-AT BUS
99999-925-100 EC
1.00
1993.7.22.
13/17
DRAWER
CHECKER
APPROVE



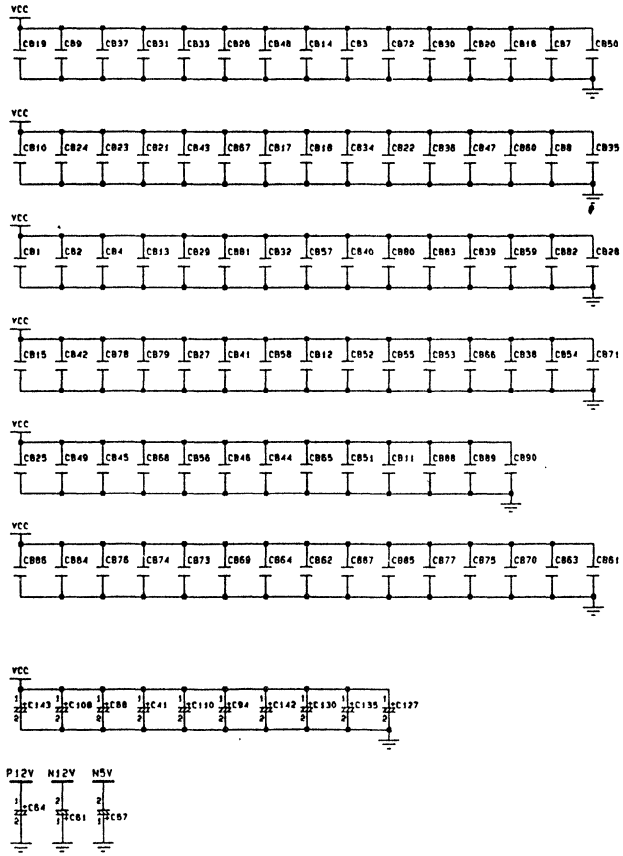
SCHEMATIC NAME	SD925E-CL-GD5426/28			
BOM NO.	99999-925-100 EC			
REV NO.	1.00	DRAWER	CHECKER	APPROVE
DATE	1993.7.26.			
SHEET NO.	14/17			

DAEDUCK ELECTRONICS CO., LTD.
ALL RIGHTS RESERVED


2 MEG OPTION FOR CL-GD5426
STANDARD 512KB (CL-GD5426/28)
MD (0: 31)
VMA (0: 8)
RAS0#
CAS2#
CAS3#
WE#
RAS0#
CAS0#
CAS1#
WE#
UP TO 1MB (CL-GD5426/28)
D (0: 31)
VD (0: 15)
NWR#
NOEL#
NOEH#
74F245
DRAM TIMING OPTIONS
MD26 MD25 MCLK
MD (25) MCLK S0 0 0 50.11Mhz
MD (26) MCLK S1 0 1 44.74Mhz
1 0 41.16Mhz
1 1 37.58Mhz
MD (27) DRAM S0 MD27
0 = HIGH PERFORMANCE
MD (28) Multiple CAS 1 = NORMAL MODE
NOTE: DRAM SPEED DEPENDS ON THE DRAM TIMING OPTIONS
REFER TO APP NOTE B7: MEMORY CONSIDERATIONS
LOCAL BUS CONFIG.
MD (21) VESA VL Bus Config.
SCHEMATIC NAME SD925E-VIDEO MEMORY
BOM NO. 99999-925-100 EC
REV NO. 1.00
DATE 1993.7.22.
SHEET NO. 15/17
DRAWER
CHECKER
APPROVE
DAEDUCK ELECTRONICS CO., LTD.
ALL RIGHTS RESERVED

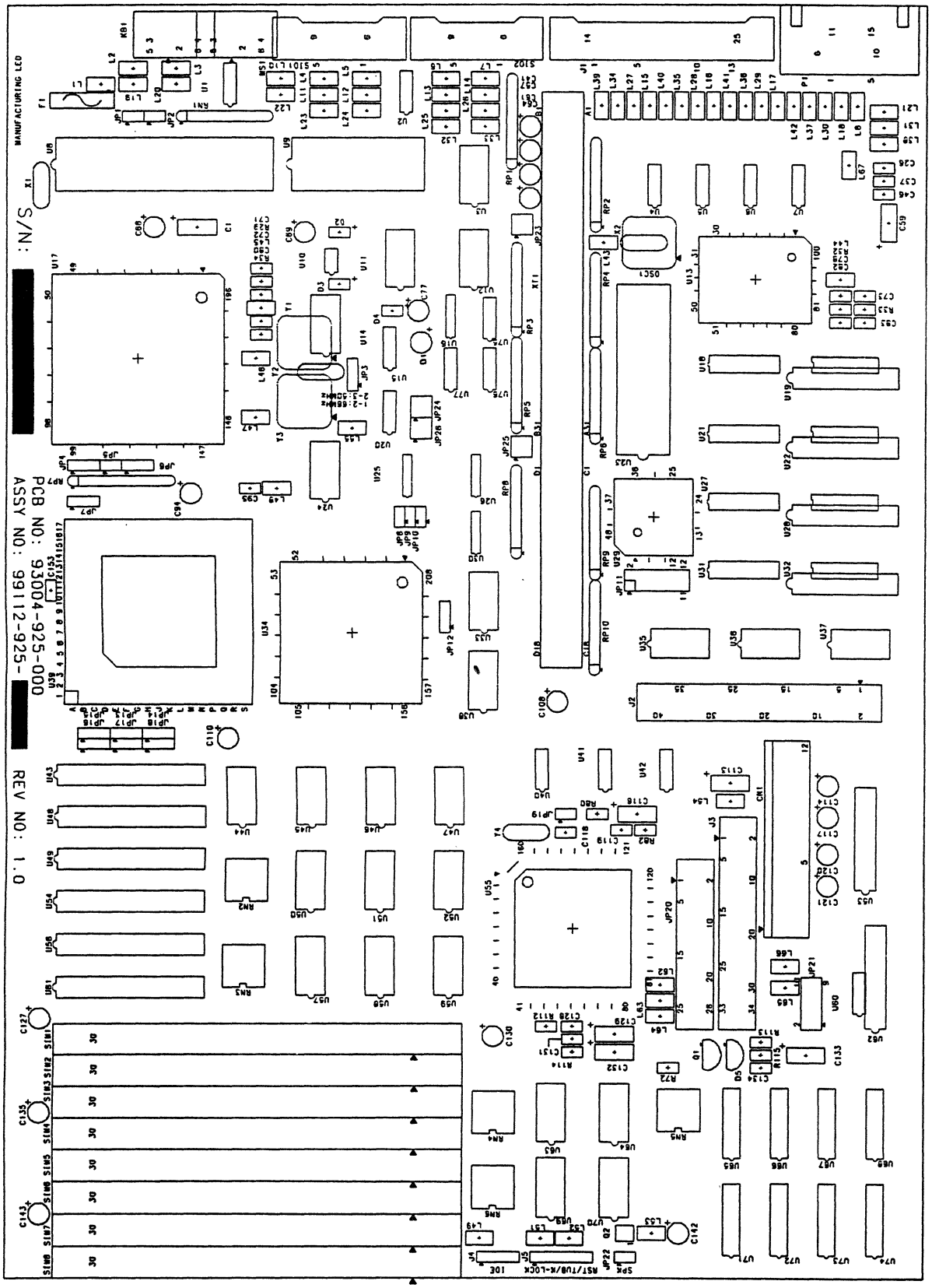

DAEDUCK ELECTRONICS CO., LTD.
ALL RIGHTS RESERVED
RED
GREEN
BLUE
15P D-sub
EDCLK*
ESYNC*
EVIDEO*
P(0:7)
JP20
DCLK
BLNK*
HSYNC
VSYNC
*Isolated GND1
IREF
DACVDD
OPTIONAL
XTAL1
XTAL2
Y4
14.318MHz
Use crystal if BOSC from the ISA bus is not used. Do not install R/C filter R84/C115 if crystal is used.
VCC
U62
PAL16L8-10
U200 : R126-8 OPEN
U115 : R126-8 SHORT
MFILVDD
GND3 *Isolated
MFILTER
VFILVDD
VFILTER
*Isolated GND2
+12V
SCHEMATIC NAME SD925E-VIDEO OUT
BOM NO. 99999-925-100 EC
REV NO. 1.00
DATE 1993.7.26.
SHEET NO. 16/17
DRAWER
CHECKER
APPROVE

DAEDUCK ELECTRONICS CO., LTD.
ALL RIGHTS RESERVED

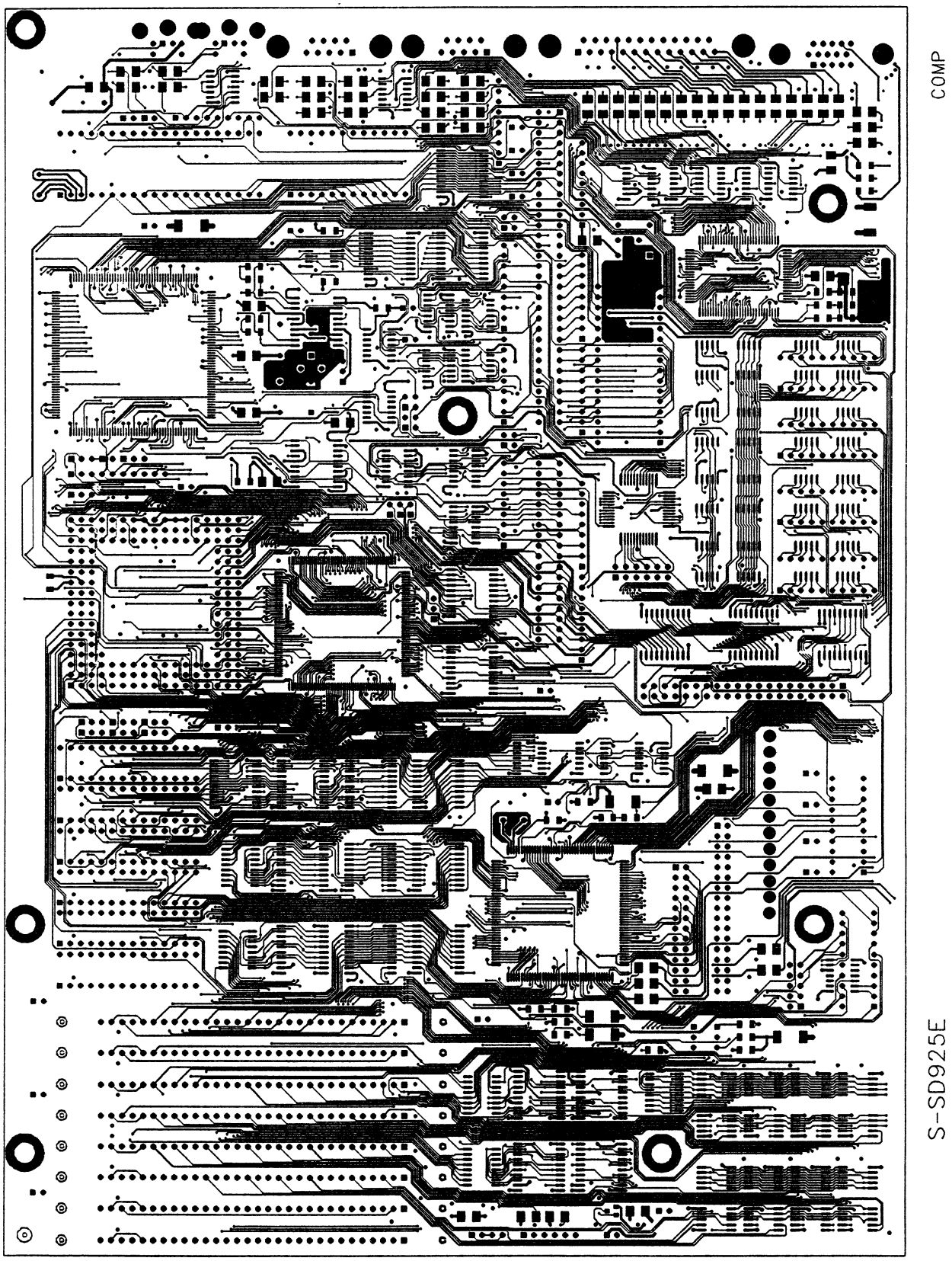


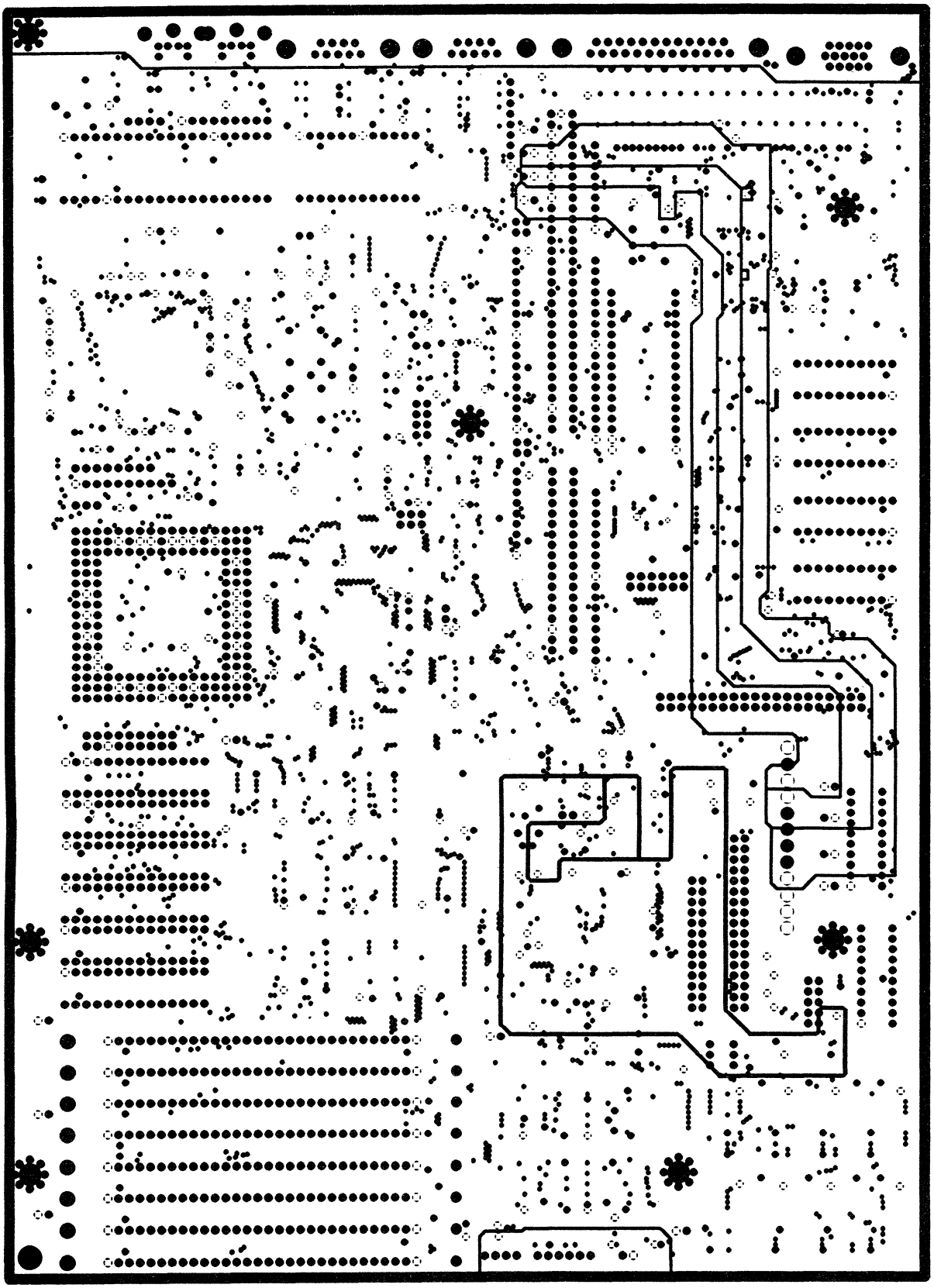
SCHEMATIC NAME	SD925E-CAP			
BOM NO.	99999-925-100 EC			
REV NO.	1.00	DRAWER	CHECKER	APPROVE
DATE	1993.7.22.			
SHEET NO.	17/17			

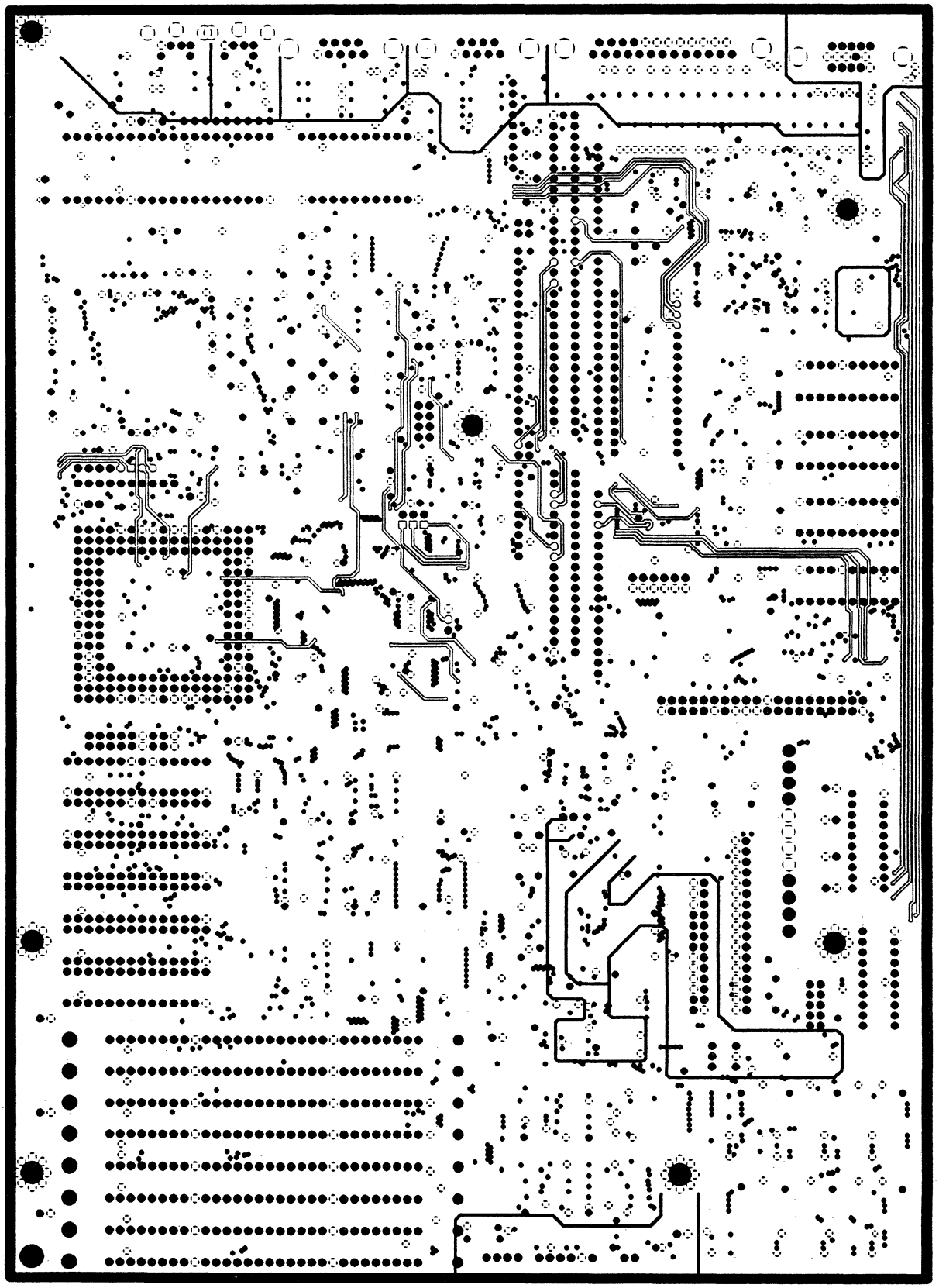
Main Board Component Layout

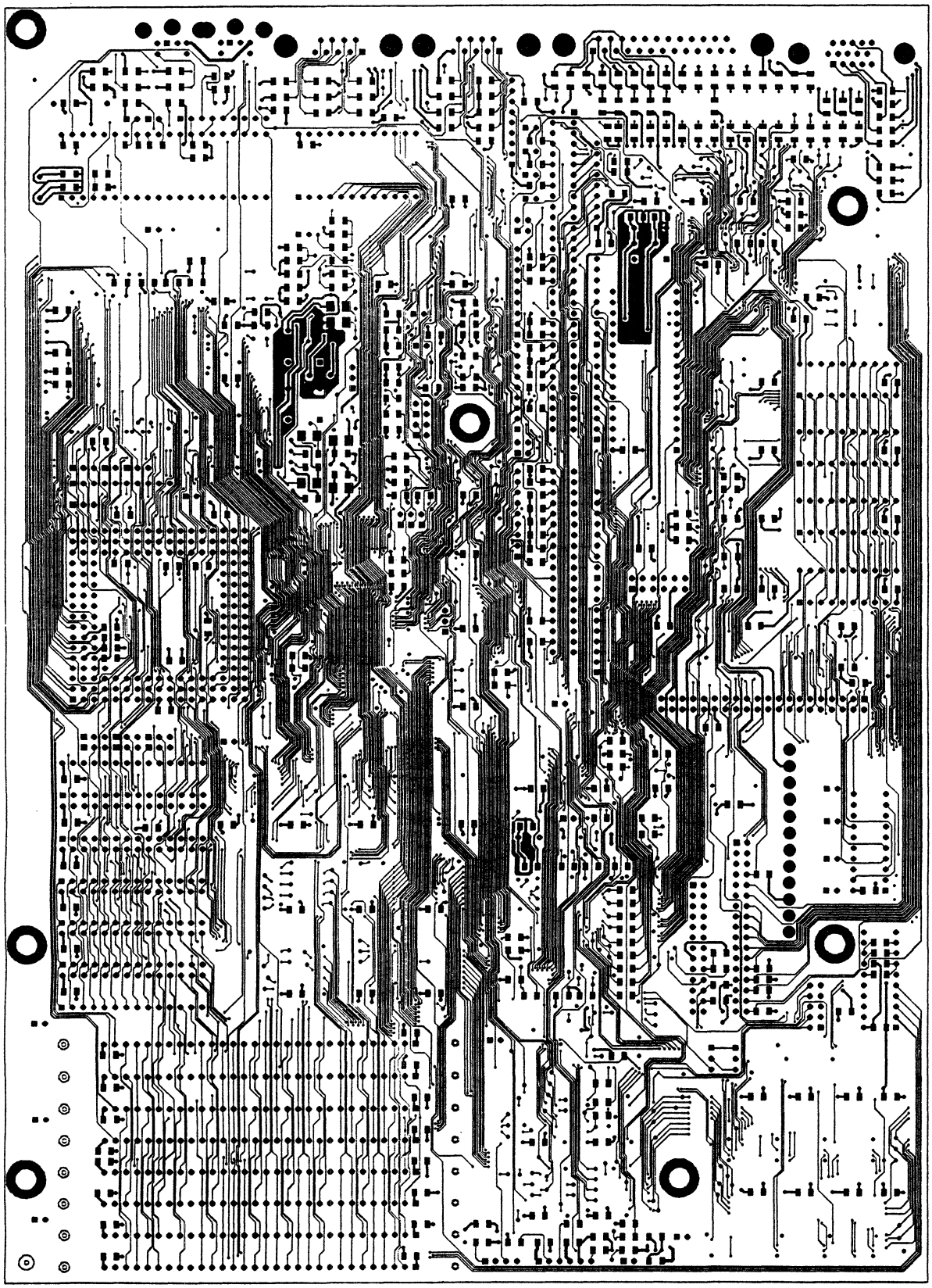


Main Board PCB Pattern

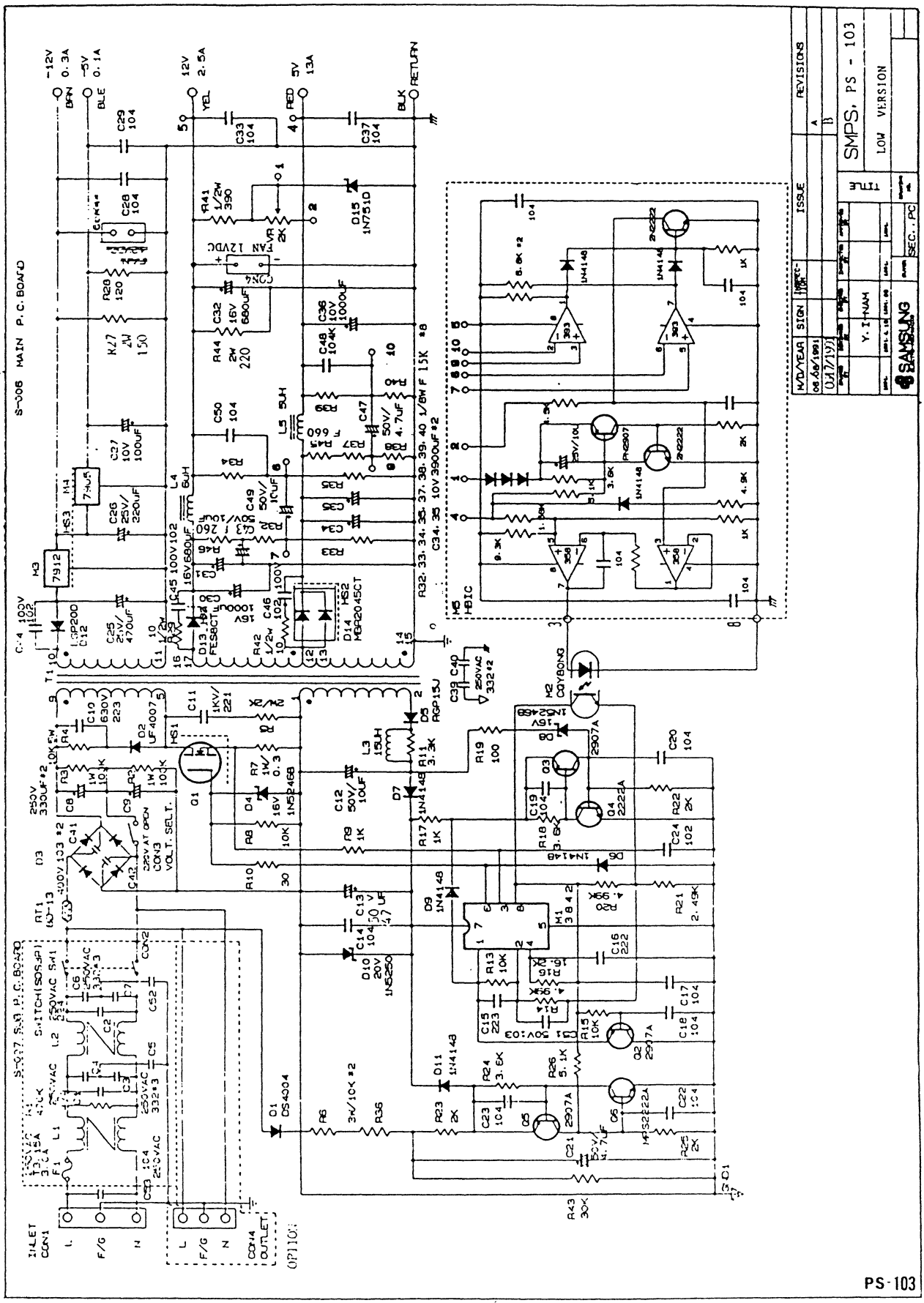


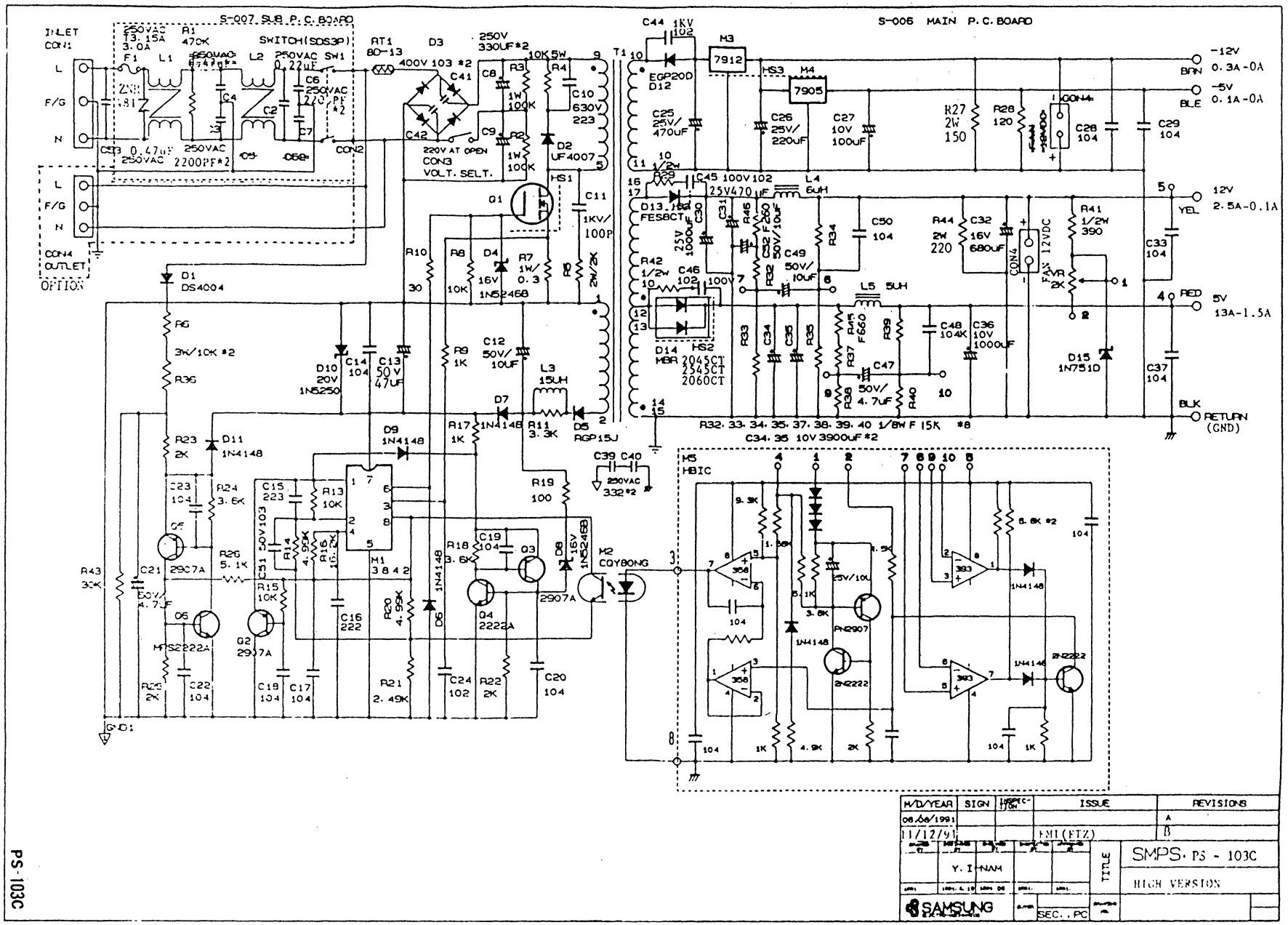

VCC
S-SD925E


GND
S-SD925E


SOLD
S-SD925E

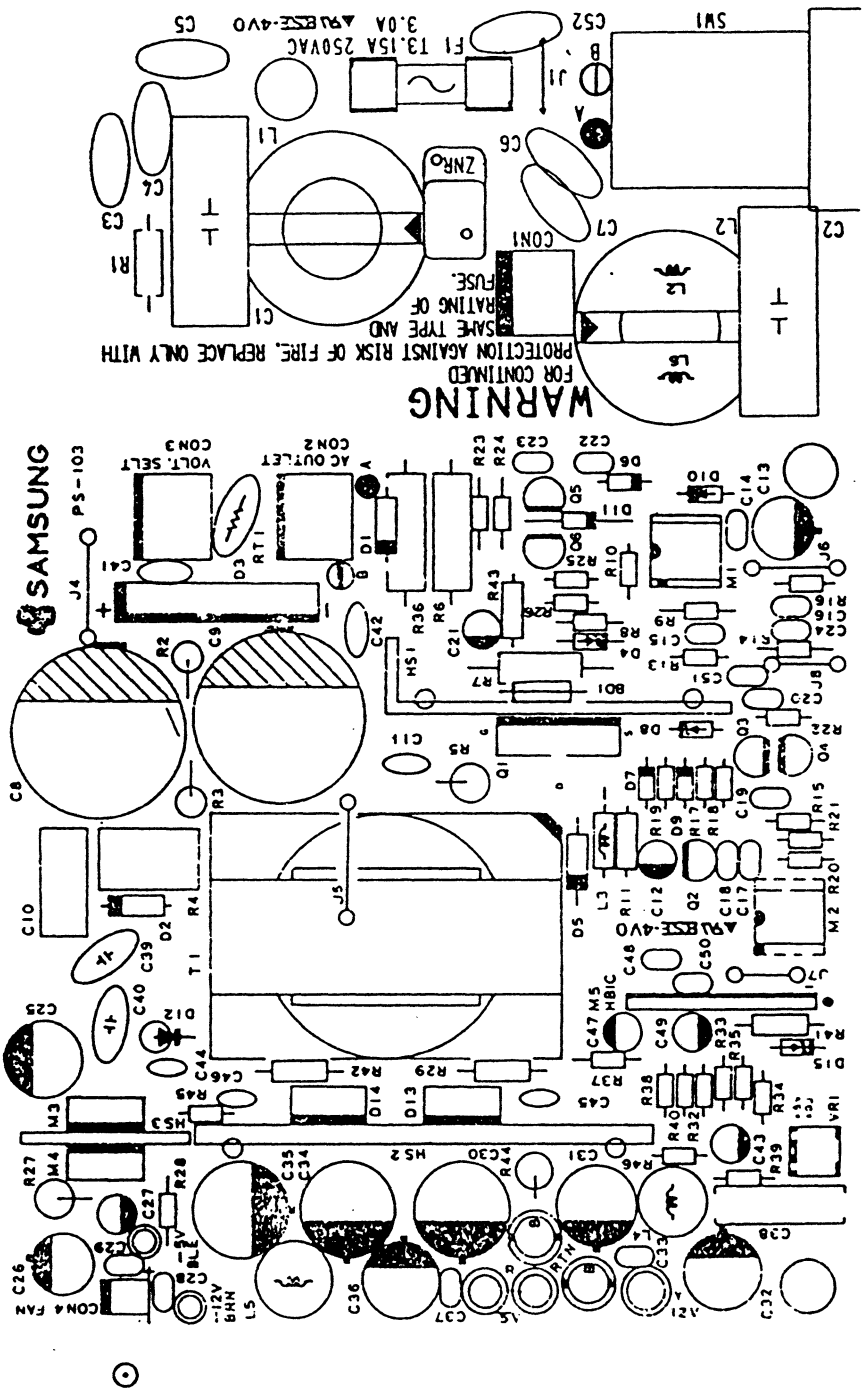
Power Supply Schematic



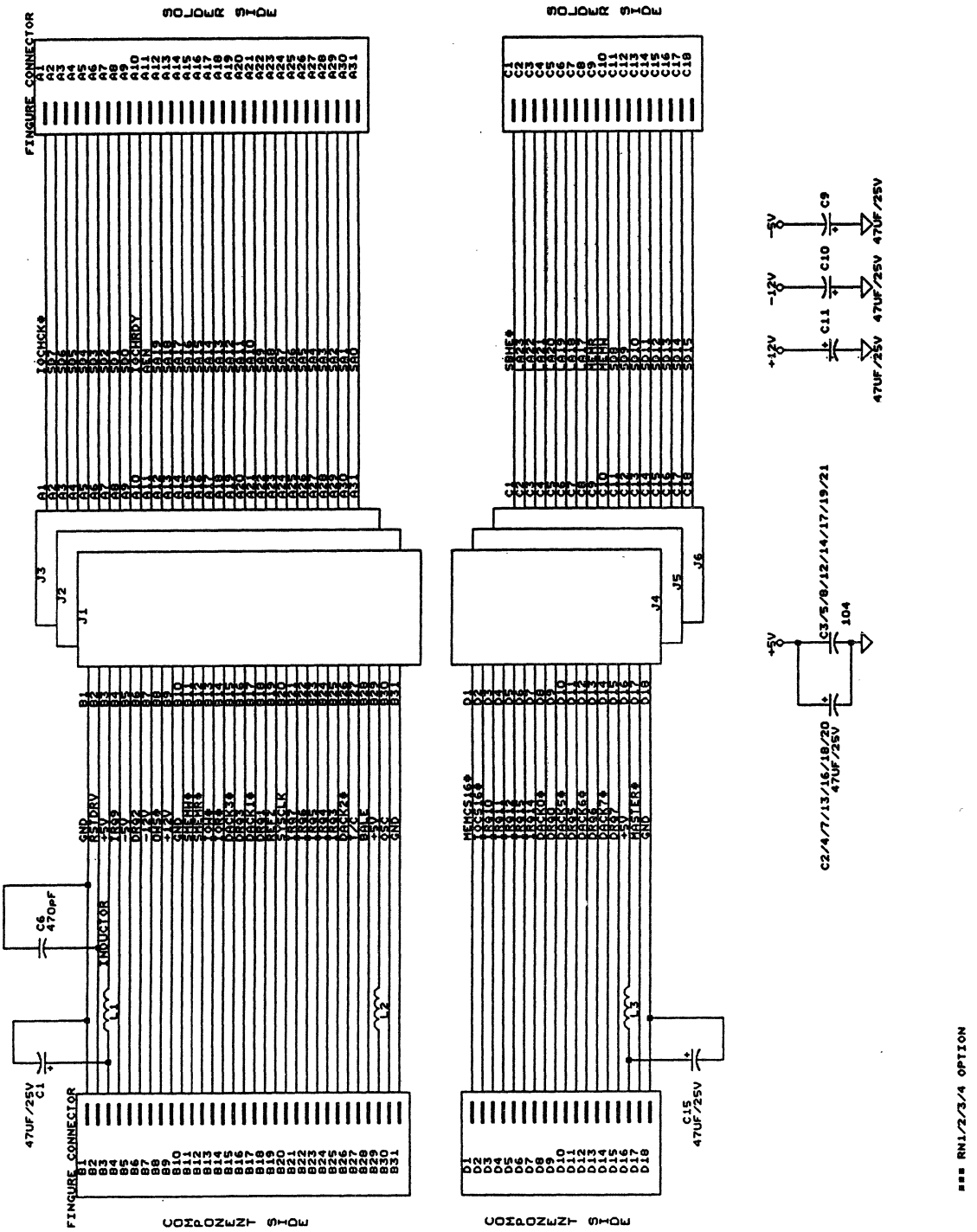

S-007 SUB P.C.BOARD
S-006 MAIN P.C.BOARD
INLET CON1
CON4 OUTLET
OPTION
SWITCH(SDS3P)
CON2
CON3 VOLT. SELT.
220V AT OPEN
HS1
HS2
HS3
M1 3842
M2 COY80NG
M3 7912
M4 7905
M5 HBIC
-12V 0.3A-0A
-5V 0.1A-0A
12V 2.5A-0.1A
5V 13A-1.5A
RETURN (GND)
SMPS. PS - 103C
HIGH VERSION
SAMSUNG
Y. I-NAM
SEC. . PC
ISSUE
REVISIONS
M/D/YEAR
SIGN
08/08/1991
11/12/91
FMI(FTZ)
TITLE

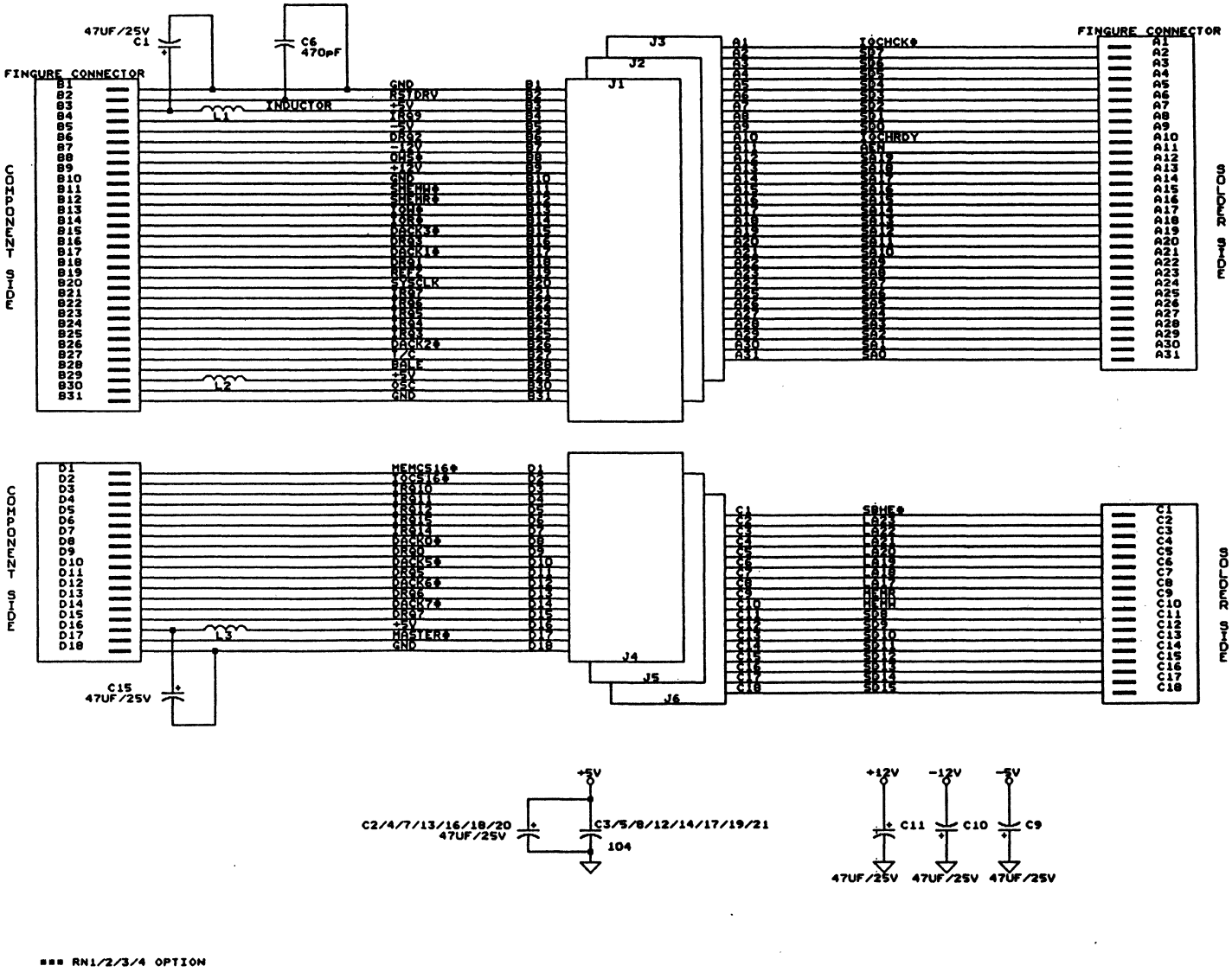
PS-103C

Power Supply Component Layout

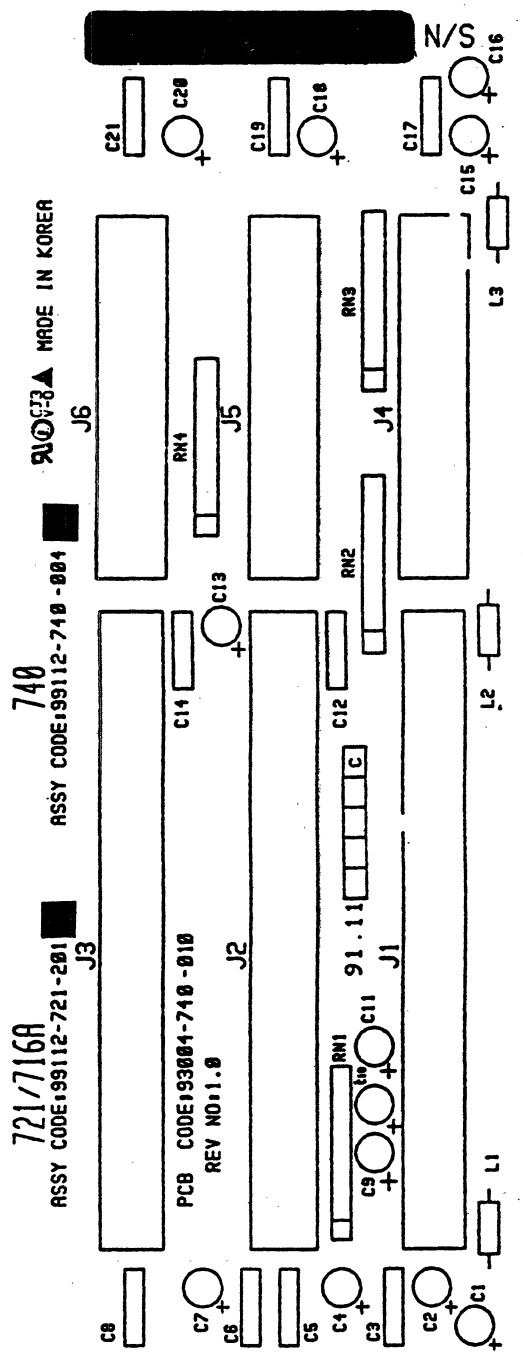


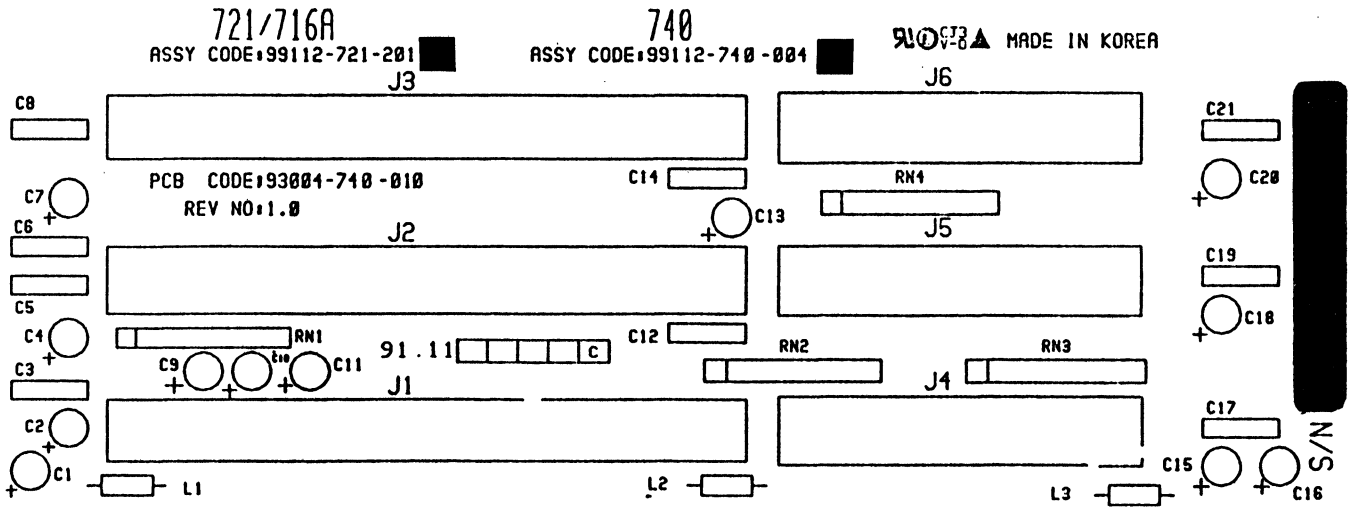
Bus Board Schematic



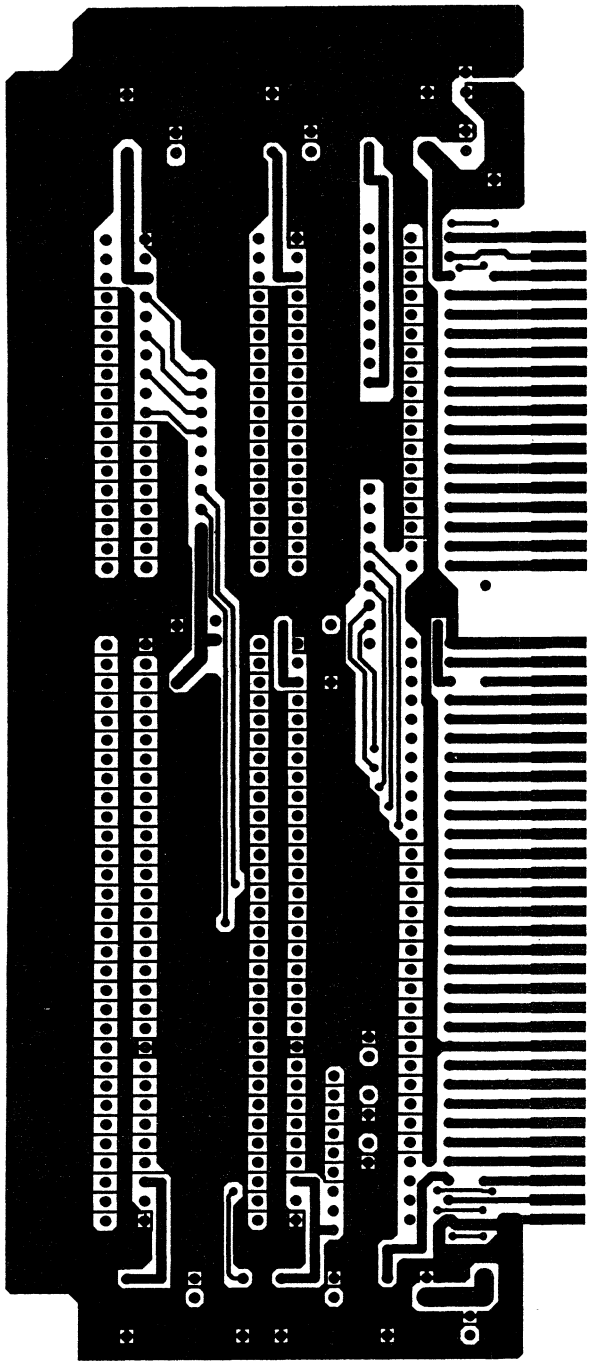

47UF/25V
C1
C6
470pF
FINGURE CONNECTOR
XINDUCTOR
L1
L2
L3
COMPONENT SIDE
SOLDER SIDE
J1
J2
J3
J4
J5
J6
C15
47UF/25V
+5V
+12V
-12V
-5V
C2/4/7/13/16/18/20
47UF/25V
C3/5/8/12/14/17/19/21
104
C11
C10
C9
47UF/25V
47UF/25V
47UF/25V
*** RN1/2/3/4 OPTION

Bus Board Component Layout

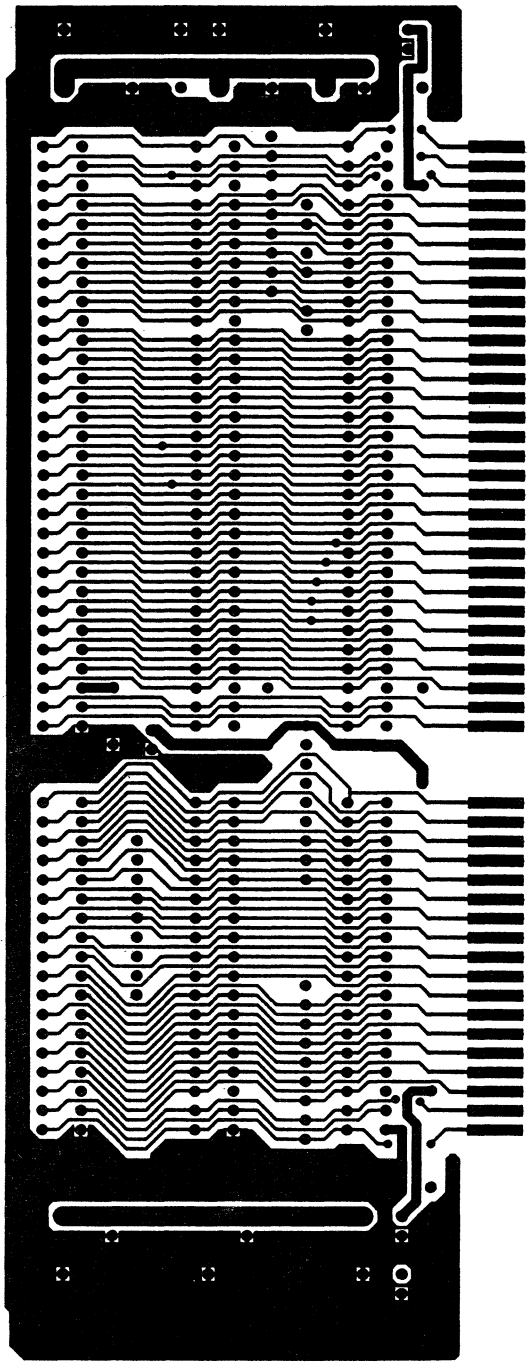



721/716A
ASSY CODE:99112-721-201
740
ASSY CODE:99112-740-004
MADE IN KOREA
J3
J6
C8
C21
PCB CODE:93001-740-010
REV NO:1.0
C14
RN4
C20
C7
C13
C6
J2
J5
C19
C5
C18
C4
RN1
91.11
C12
RN2
RN3
C9
C11
J1
J4
C3
C17
C2
C15
C1
L1
L2
L3
C16
N/S

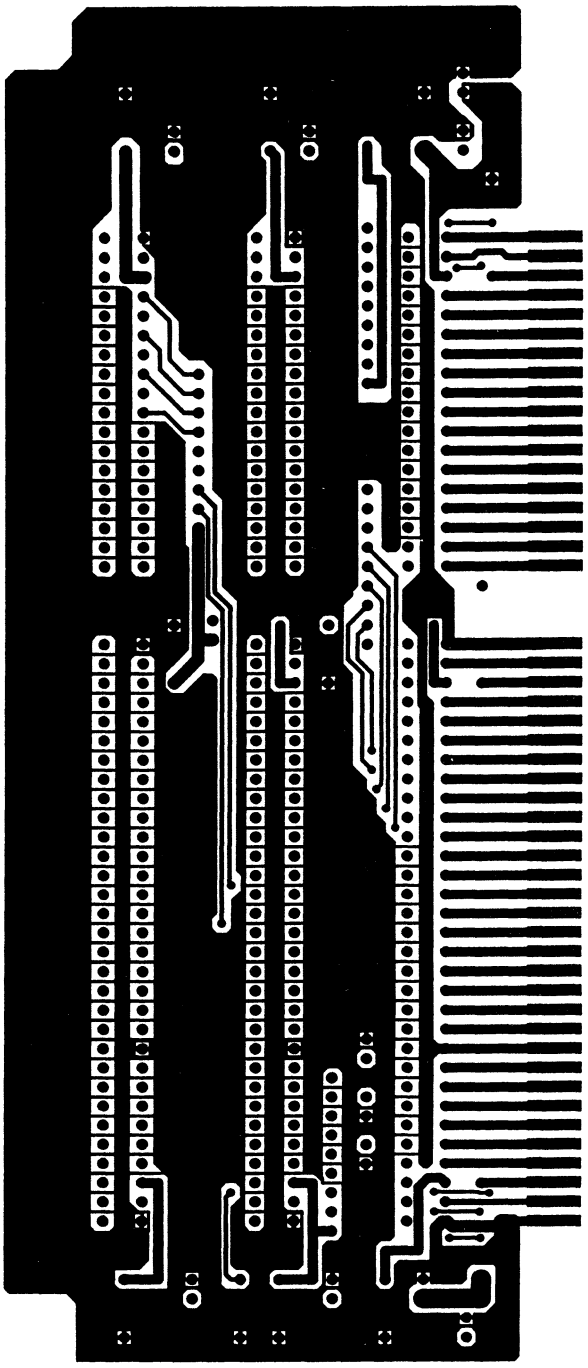
Bus Board PCB Pattem



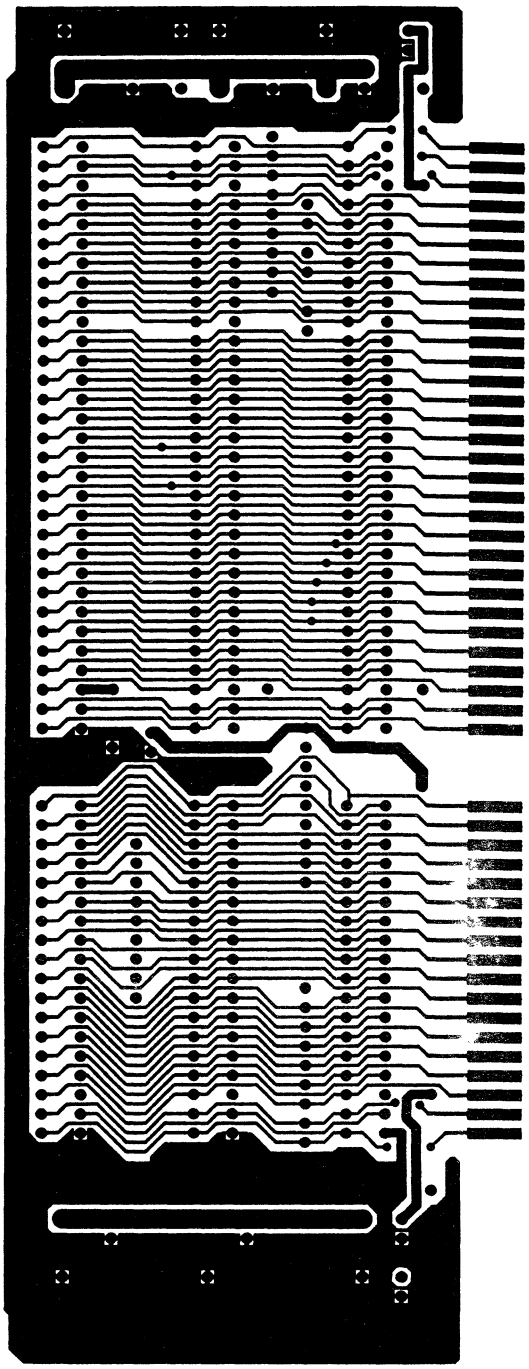
COMPONENT SIDE ARTWORK



SOLDER SIDE ARTWORK



COMPONENT SIDE ARTWORK



SOLDER SIDE ARTWORK

Chapter 6. Parts List

Main Board Parts List
Power Supply Parts List

Main Board Parts List

Lvl	PART NUMBER	CC	SPECIFICATION	RQTY-PER	REF DESN	DATE
1	99101-925Q001		ASSY-BOTTOM;SD925Q S	1.000		930426
2	97088-130-062		SCREW-MACHINE;BH,+,M3.0 S	8.000		930426
2	97458-230-062		SCREW-TAPTITE;BH,+S,M3. S	2.000		930426
2	97693-900-801		BADGE-REAR,B;P.C SHEET S	1.000		930426
2	98901-902-120		CHASSIS-ASSY;EGI T1.0 R S	0.000		930428
2	98901-902-130		CHASSIS-ASSY,;E.G.1 T1. S	1.000		930506
1	99102-62A-001		ASSY-COVER;SD620A/716A/ T	1.000		930318
2	96121-907-210		CHASSIS-COVER;EGI T1.0, T	1.000		901108
2	97088-130-062		SCREW-MACHINE;BH,+,M3.0 T	3.000		900101
1#	99103-925Q003		ASSY-BEZEL&COVER;DM486S T	1.000		930318
2	96613-919-410		LEVER;ABS VH0800-C7096 T	1.000		930514
3	90742-185-069		RESIN-ABS;VH-0800 C7096	0.024		900412
2	96674-902-010		SPRING-POWER;SUS-WPA PI T	2.000		930318
2	97408-130-101		SCREW-TAPTITE;PH,+B,M3. T	3.000		930318
2	97624-905-410		KNOB-POWER;VH-0800 C709 T	1.000		930318
3	90742-185-069		RESIN-ABS;VH-0800 C7096	0.002		900412
2	97624-973-010		KNOB;RESET ,VH-0800 T	1.000		930318
2	97654-901-611		LENS;ACRYL NATURAL(LED) T	3.000		930318
2	98023-900-390		BADGE;P.C SHEET T0.25 T	1.000		930318
2	98901-902-360		BEZEL-ASSY;ABS VH0800D- T	1.000	COVER	930706
1	99112-000-501		ASSY-OSC CLOCK;OSC 50MH E	1.000		930721
2	93354-100-400		SOCKET-IC;DIP-THD ,4P E	1.000	Y1	930721
2	94049-903-941		CORE-FERRITE;2743019447 V	2.000	L46-L47	930721
2	94539-014-319		OSC-CLOCK;14.31818 M,50 E	1.000	Y3	930721
2	94539-050-003		OSC-CLOCK;50.000MHZ ,50 E	1.000	Y1	930721
2	96634-901-510		BAND-WIRE;100MM E	1.000		930721
1#	99112-620-103		ASSY-POWER CORD;115V,US T	1.000		930318
2	93053-861-620		POWER-CORD;PV0305CBS6F1 T	1.000		910424
2	98654-906-010		PE BAG; ,HDPE T	1.000		910816
1	99112-740-004		ASSY-BUS;D386S/25 X	1.000		930521
2	91302-104-150	01	C-CERAMIC MONO;0.1uF ,+ X	6.000	C3,5,8,12,14,17	911008
2	91302-104-150	02	C-CERAMIC MONO;0.1uF ,+ X	2.000	C19,21	911008
2	91302-471-356		C-CERAMIC MONO;470pF ,1 X	1.000	C6	911008
2	91603-904-472	01	C-ELECTRONIC;47uF ,20% X	7.000	CE1,2,4,7,9-11	911008
2	91603-904-472	02	C-ELECTRONIC;47uF ,20% X	5.000	CE13,15,16,18,20	911008
2	93004-740-010		PCB;BUS-B/D 18,X75MM2LA X	1.000		911128
2	93340-798-050		CONN-C/E;BMR-THD ,98P X	3.000	J1-3	911008
2	94049-901-611		CORE-FERRITE;L5RH3 (NAM X	3.000	L1-3	911008
1#	99112-925-128		ASSY-CACHE MEM 128K ;32 E	1.000		930402
2	92113-500-886		IC-SRAM;6865BP-15 ,8K * E	2.000		930628
2	92113-503-285		IC-SRAM;68257BP-20,32K E	4.000		930628
1#	99112-925-612		ASSY-MEM 44C256+4EA ;SD E	1.000		930403
2	92113-425-642		IC-DRAM;44C256 ,256K E	4.000		930628
1	99112-925-900		ASSY-MOTHER B/D;SD925E E	1.000		930609
2	91061-472-190		R-NETWORK SIP;4.7K ,5% E	7.000	RN1,RP1-RP6	930609
2	91061-472-190	01	R-NETWORK SIP;4.7K ,5% E	3.000	RP8-RP9	930609
2	91069-101-190		R-NETWORK SIP;4.7K ,5% E	1.000	RP7	930609
2	91609-010-230		C-ELECTRONIC;10uF ,20% E	4.000	C41,C57,C61,C64	930609
2	91609-010-230	01	C-ELECTRONIC;10uF ,20% E	3.000	C114,C117,C120	930609

Lvl	PART NUMBER	CC	SPECIFICATION	RQTY-PER	REF DESN	DATE
2	91609-010-230	02	C-ELECTRONIC:10uF ,20% E	1.000	C121	930609
2	91609-010-660		C-ELECTRONIC:10uF ,20% E	4.000	C55,C68,C69,C77	930609
2	91609-010-660	01	C-ELECTRONIC:10uF ,20% E	3.000	C94,C108,C110	930609
2	91609-010-660	02	C-ELECTRONIC:10uF ,20% E	3.000	C127,C130,C135	930609
2	91609-010-660	03	C-ELECTRONIC:10uF ,20% E	2.000	C142,C143	930609
2	92109-400-050		IC-CUSTOM:DS1287 ,DI E	1.000	U9	930609
2	92113-212-884		IC-EPROM:27C010 ,128 E	1.000	U23	930609
2	92113-616-085		IC-PAL:16L8B ,16*8 E	1.000	U53	930708
2	92115-180-422		IC-CPU:P8042-1.03,DIP-4 E	1.000	U8	930609
2	92119-204-310		IC-LINEAR:TL431 ,TO E	1.000	D5	930609
2	92139-401-360		TR-GENERAL:2N3904 ,T E	1.000	Q1	930609
2	92309-110-010		LED:SLR34MC,ROUND,GREEN E	1.000	D1	930609
2	93310-021-260		CONN-HEADER:BM4W-THD , E	1.000	JP20	930610
2	93313-021-600		CONN-SOCKET:SIMM-THD , E	4.000	SIM1-SIM8	930609
2	93340-102-080		CONN-HEADER:BM4W-THD , E	1.000	JP22	930609
2	93340-106-050		CONN-HEADER:BM4W-THD , E	1.000	J5	930609
2	93340-110-040		CONN-HEADER:BM1W-THD , E	1.000	CN1	930628
2	93340-502-120		CONN-SHUNT:JUMPER ,2 E	30.000		930610
2	93340-798-050		CONN-C/E:BMR-THD ,98P E	1.000	XT1,AT1	930609
2	93341-002-100		CONN-HEADER:BMNW-THD , E	5.000	JP1,JP2,JP8-JP10	930609
2	93341-002-100	01	CONN-HEADER:BMNW-THD , E	2.000	JP5,JP19	930726
2	93341-003-080		CONN-HEADER:BMNW-THD , E	3.000	JP4,JP6,JP7	930721
2	93341-003-080	01	CONN-HEADER:BMNW-THD , E	3.000	JP12-JP14	930609
2	93341-003-080	02	CONN-HEADER:BMNW-THD , E	4.000	JP15,JP16-JP18	930726
2	93345-013-090		CONN-DSUB:BMP-THD ,9P E	2.000	SIO1,SIO2	930609
2	93345-017-152		CONN-DSUB:BMR-THD ,15 E	1.000	P1	930609
2	93345-017-250		CONN-DSUB:BMR-THD ,25 E	1.000	J1	930609
2	93345-021-100		CONN-HEADER:BMNW-THD , E	1.000	JP21	930609
2	93345-023-041		CONN-HEADER:BMNW-THD , E	1.000	J4	930609
2	93345-025-341		CONN-HEADER:BM4W-THD , E	1.000	J3	930609
2	93345-025-401		CONN-HEADER:BM4W-THD , E	1.000	J2	930609
2	93345-051-002		CONN-JACK:DIN-THD ,6P E	2.000	KB1,MS1	930609
2	93354-102-800		SOCKET-IC:DIP-THD ,28 E	4.000	U43,U48,U49,U54	930609
2	93354-102-800	01	SOCKET-IC:DIP-THD ,28 E	2.000	U56,U61	930609
2	93354-120-030		SOCKET-IC:DIP-THD ,20 E	4.000	U19,U22,U28,U32	930609
2	93354-120-030	01	SOCKET-IC:DIP-THD ,20 E	1.000	U53	930609
2	93354-124-010		SOCKET-IC:DIP-THD ,24 E	1.000	U9	930609
2	93354-132-070		SOCKET-IC:DIP-THD ,32 E	1.000	U23	930609
2	93354-140-010		SOCKET-IC:DIP-THD ,40 E	1.000	U8	930609
2	93354-416-910		SOCKET-IC:PGA-THDLIF,16 E	1.000	U39	930609
2	94539-014-318		CRYSTAL:14.31818M ,30PP E	1.000	Y4	930721
2	94539-024-000		OSC-CLOCK:24.000MHZ ,50 E	1.000	OSC1	930609
2	94539-915-600		CRYSTAL:12 MHZ ,50PP E	1.000	X1	930609
2	94709-902-710		FUSE:251004,PICO E	1.000	L9	930609
2	99112-925-800		ASSY-MOTHER B/D:SD925E V	1.000		930608
3	91068-100-560		R-NETWORK SOP:10 ,2% V	5.000	RN2-RN6	930609
3	91083-000-150		R-CARBON CHIP:0 ,5% V	2.000	C66,R76	930618
3	91083-000-150	01	R-CARBON CHIP:0 ,5% V	4.000	R77,R95,R96,R102	930609
3	91083-000-150	02	R-CARBON CHIP:0 ,5% V	4.000	R23,R31,R40,R60	930609
3	91083-000-150	03	R-CARBON CHIP:0 ,5% V	2.000	R61,R63	930609
3	91083-100-150		R-CARBOM CHIP:10 ,5% V	5.000	R43,R45-R47,R64	930609
3	91083-100-150	01	R-CARBOM CHIP:10 ,5% V	5.000	R68-R69,R116-118	930609

Lvl	PART NUMBER	CC	SPECIFICATION	RQTY-PER	REF DESN	DATE
3	91083-101-150		R-CARBON CHIP:100 ,5% V	1.000	R106	930609
3	91083-102-150		R-CARBON CHIP:1K ,5% V	3.000	R70,R72,R115	930608
3	91083-102-150	01	R-CARBON CHIP:1K ,5% V	5.000	R1,R10-R12,R14	930609
3	91083-102-150	02	R-CARBON CHIP:1K ,5% V	4.000	R19,R25,R30,R36	930609
3	91083-102-150	03	R-CARBON CHIP:1K ,5% V	4.000	R38,R67,R71,R73	930609
3	91083-102-150	04	R-CARBON CHIP:1K ,5% V	4.000	R78,R93,R98,R119	930609
3	91083-103-150		R-CARBON CHIP:10K ,5% V	4.000	R16-R18,R20	930609
3	91083-104-150		R-CARBON CHIP:100K ,5% V	1.000	R22	930609
3	91083-151-150		R-CARBON CHIP:150 ,5% V	4.000	R4,R6,R9,R88	930609
3	91083-151-150	01	R-CARBON CHIP:150 ,5% V	3.000	R101,R105,R109	930609
3	91083-151-150	02	R-CARBON CHIP:150 ,5% V	3.000	R111,R122,R123	930609
3	91083-151-150	03	R-CARBON CHIP:150 ,5% V	1.000	R124	930609
3	91083-202-151	01	R-CARBON CHIP:2K ,5% V	2.000	R120,R121	930609
3	91083-220-150		R-CARBON CHIP:22 ,5% V	4.000	R81,R83,R86,R87	930609
3	91083-220-150	01	R-CARBON CHIP:22 ,5% V	6.000	R89-R92,R94,R97	930609
3	91083-220-150	02	R-CARBON CHIP:22 ,5% V	3.000	R99,R103,R108	930609
3	91083-222-150		R-CARBON CHIP:2.2K ,5% V	4.000	R24,R44,R48,R51	930609
3	91083-222-150	01	R-CARBON CHIP:2.2K ,5% V	1.000	R53	930609
3	91083-330-150		R-CARBON CHIP:33 ,5% V	2.000	R80,R112	930608
3	91083-330-150	01	R-CARBON CHIP:33 ,5% V	4.000	R15,R79,R85,R100	930609
3	91083-330-150	02	R-CARBON CHIP:33 ,5% V	3.000	R104,R110,R125	930609
3	91083-331-150		R-CARBON CHIP:330 ,5% V	4.000	R13,R49,R52,R66	930609
3	91083-361-150		R-CARBON CHIP:360 ,5% V	1.000	R113	930608
3	91083-472-150		R-CARBON CHIP:4.7K ,5% V	5.000	R2,R3,R5,R8,R21	930609
3	91083-472-150	01	R-CARBON CHIP:4.7K ,5% V	4.000	R26-R28,R35,R55	930609
3	91083-472-150	02	R-CARBON CHIP:4.7K ,5% V	3.000	R127,R129,R134	930728
3	91083-472-150	03	R-CARBON CHIP:4.7K ,5% V	1.000	R135	930728
3	91083-561-150		R-CARBON CHIP:560 ,5% V	1.000	R33	930608
3	91083-561-150	01	R-CARBON CHIP:560 ,5% V	1.000	R7	930609
3	91083-562-150		R-CARBON CHIP:5.6K ,5% V	1.000	R32	930608
3	91083-682-150		R-CARBON CHIP:6.8K ,5% V	4.000	R50,R54,R62,R65	930609
3	91083-682-150	01	R-CARBON CHIP:6.8K ,5% V	1.000	R107	930609
3	91083-750-110		R-CARBON CHIP:75 ,1% V	2.000	R82,R114	930609
3	91301-100-250	01	C-CERAMIC CHIP:10pF ,5 V	3.000	C92,C93,C101	930609
3	91301-100-250	02	C-CERAMIC CHIP:10pF ,5 V	2.000	C104,C106	930609
3	91301-101-752		C-CERAMIC CHIP:100pF ,5 V	5.000	C49,C81,C84-C86	930609
3	91301-101-752	01	C-CERAMIC CHIP:100pF ,5 V	6.000	C88,C96-C100	930609
3	91301-101-752	02	C-CERAMIC CHIP:100pF ,5 V	1.000	C102	930609
3	91301-104-310		C-CERAMIC CHIP:0.1uF ,1 V	2.000	C95,C118	930721
3	91301-104-310	01	C-CERAMIC CHIP:0.1uF ,1 V	3.000	C119,C128,C131	930608
3	91301-104-310	02	C-CERAMIC CHIP:0.1uF ,1 V	1.000	C134	930608
3	91301-104-310	03	C-CERAMIC CHIP:0.1uF ,1 V	4.000	C2,C12,C63,C74	930609
3	91301-104-310	04	C-CERAMIC CHIP:0.1uF ,1 V	2.000	C76,C111	930721
3	91301-104-310	05	C-CERAMIC CHIP:0.1uF ,1 V	3.000	C112,C122,C144	930609
3	91301-104-310	06	C-CERAMIC CHIP:0.1uF ,1 V	3.000	C124-C126	930609
3	91301-104-310	07	C-CERAMIC CHIP:0.1uF ,1 V	5.000	C136,C138-C141	930726
3	91301-104-310	08	C-CERAMIC CHIP:0.1uF ,1 V	87.000	CB1-CB87	930609
3	91301-104-310	09	C-CERAMIC CHIP:0.1uF ,1 V	6.000	C149,C150-C154	930728
3	91301-104-310	10	C-CERAMIC CHIP:0.1uF ,1 V	8.000	C155-C161,C176	930726
3	91301-123-750		C-CERAMIC CHIP:12nF ,1 V	1.000	C83	930608
3	91301-150-757		C-CERAMIC CHIP:15pF ,5 V	2.000	C60,C62	930609
3	91301-153-750		C-CERAMIC CHIP:15nF ,1 V	1.000	C82	930608

Lvl	PART NUMBER	CC	SPECIFICATION	RQTY-PER	REF DESN	DATE
3	91301-221-757		C-CERAMIC CHIP:220pF ,5 V	4.000	C11,C18,C19,C20	930609
3	91301-221-757	01	C-CERAMIC CHIP:220pF ,5 V	6.000	C21,C23,C33-C36	930609
3	91301-221-757	02	C-CERAMIC CHIP:220pF ,5 V	8.000	C42-C45,C50-C53	930609
3	91301-221-757	03	C-CERAMIC CHIP:220pF ,5 V	2.000	C105,C109	930618
3	91301-221-757	04	C-CERAMIC CHIP:220pF ,5 V	17.000	C162-C180	930726
3	91301-331-756		C-CERAMIC CHIP:330pF ,5 V	1.000	C91	930609
3	91301-333-357		C-CERAMIC CHIP:33nF ,1 V	1.000	C78	930608
3	91301-470-757		C-CERAMIC CHIP:47pF ,5 V	12.000	C3-C9,C13-C17	930609
3	91301-470-757	01	C-CERAMIC CHIP:47pF ,5 V	10.000	C22,C24-C32	930609
3	91301-470-757	02	C-CERAMIC CHIP:47pF ,5 V	7.000	C37-C40,C46-C48	930609
3	91301-470-757	03	C-CERAMIC CHIP:47pF ,5 V	3.000	C56,C58,C103	930609
3	91301-470-757	04	C-CERAMIC CHIP:47pF ,5 V	2.000	C107,C123	930609
3	91301-471-757		C-CERAMIC CHIP:470pF ,5 V	1.000	C87	930609
3	91301-511-750		C-CERAMIC CHIP:510pF ,5 V	1.000	C73	930608
3	91301-560-756		C-CERAMIC CHIP:56pF ,5 V	5.000	C184-C188	930726
3	91629-106-640		C-TANTAL CHIP:10uF ,10 V	4.000	C1,C10,C59,C113	930608
3	91629-106-640	01	C-TANTAL CHIP:10uF ,10 V	2.000	C129,C133	930608
3	91629-225-330		C-TANTAL CHIP:2.2uF ,10 V	2.000	C116,C132	930608
3	92109-440-020		IC-TTL:74F02 ,SOP-1 V	1.000	U42	930609
3	92109-441-510		IC-TTL:74F151 ,SOP-1 V	3.000	U16,U26,U30	930609
3	92109-510-060		IC-TTL:7406D ,SOP-1 V	1.000	U1	930608
3	92109-520-041		IC-TTL:74LS04 ,SOP-1 V	1.000	U15	930609
3	92109-520-740		IC-TTL:74LS74A ,SOP-1 V	3.000	U75-U77	930728
3	92109-522-440		IC-TTL:74LS244 ,SOP-W V	1.000	U37	930609
3	92109-522-450		IC-TTL:74LS245 ,SOP-W V	2.000	U35,U36	930609
3	92109-540-040		IC-TTL:74F04 ,SOP-1 V	1.000	U40	930609
3	92109-540-320		IC-TTL:74F32 ,SOP-1 V	1.000	U60	930609
3	92109-541-250		IC-TTL:74F125A ,SOP-1 V	1.000	U41	930609
3	92109-541-260		IC-TTL:74F126 SOP-1 V	1.000	U20	930609
3	92109-542-440		IC-TTL:74F244 ,SOP-2 V	2.000	U38,U46	930609
3	92109-542-440	01	IC-TTL:74F244 ,SOP-2 V	4.000	U24,U50,U57,U63	930609
3	92109-542-440	02	IC-TTL:74F244 ,SOP-2 V	3.000	U64,U69,U70	930609
3	92109-542-455		IC-TTL:74F245 ,SOP-2 V	4.000	U3,U11,U12,U33	930609
3	92109-542-455	01	IC-TTL:74F245 ,SOP-2 V	3.000	U44,U45,U47	930609
3	92109-542-455	02	IC-TTL:74F245 ,SOP-2 V	4.000	U51,U52,U58,U59	930609
3	92109-911-841		IC-CUSTOM:PC87310A ,PQ V	1.000	U13	930609
3	92111-751-882		IC-INTERFACE:75188 V	2.000	U4,U5	930608
3	92111-751-892		IC-INTERFACE:75189A V	3.000	U2,U6,U7	930608
3	92113-425-647		IC-DRAM:44C256C ,256K V	4.000	U18,U21,U27,U31	930608
3	92113-461-041		IC-DRAM:44C1000A ,1M*4 V	8.000	U65-U68,U71-U74	930608
3	92115-100-250		IC-CPU:80486SX/25,PQFP- V	1.000	U17	930609
3	92115-543-000		IC-CUSTOM:85C460 ,PQ V	1.000	U34	930609
3	92115-569-542		IC-CUSTOM:GD5426 ,PQ V	1.000	U55	930609
3	92139-239-041		TR-GENERAL:MMBT3904 ,S V	1.000	Q2	930608
3	92169-341-483		DIODE-SWITCHING:MMBD414 V	3.000	D2-D4	930608
3	92210-303-930		TR-POWER:LM393 ,SOP V	1.000	U10	930609
3	93004-925-000		PCB:306*219*1.6(4LAY) V	1.000		930609
3	93345-021-041		CONN-HEADER:BMNW-THD , V	4.000	JP23-JP26	930728
3	94049-903-941		CORE-FERRITE:2743019447 V	4.000	L1,L21,L31,L38	930609
3	94049-903-941	01	CORE-FERRITE:2743019447 V	3.000	L43,L44,L48	930609
3	94049-903-941	02	CORE-FERRITE:2743019447 V	4.000	L49,L51-L53	930726
3	94049-903-941	03	CORE-FERRITE:2743019447 V	1.000	L56	930726

Lvl	PART NUMBER	CC	SPECIFICATION	RQTY-PER	REF DESN	DATE
3	94049-903-960		CORE-FERRITE:HF50ACB322 V	18.000	L2-L8,L10-L20	930628
3	94049-903-960	01	CORE-FERRITE:HF50ACB322 V	15.000	L22-L30,L32-L37	930609
3	94049-903-960	02	CORE-FERRITE:HF50ACB322 V	5.000	L39-L42,L54	930726
3	94049-903-960	03	CORE-FERRITE:HF50ACB322 V	10.000	L57-L66	930726
1#	99113-740-001		ASSY-KBD:SEM-K20S-1 US T	1.000		930318
2	93550-274-030		KBD-ASSY:SEM-K20S-US T	1.000		911227
2	98712-906-011		CUSHION-KBD:E.P.S C=0. T	1.000		921125
1	99114-462-003		ASSY-HARNESS SPEAKER:SP X	1.000		930318
2	93053-407-510		SPEAKER HARNESS-ASSY:SP S	1.000		920228
2	94209-901-610		SPEAKER:42TH01D,32 OHM, S	1.000		920901
2	96674-903-210		SPRING-SPEAKER:SUS DIA S	0.000		930612
1	99114-925-001		HARNESS:FDD,HDD,FEATURE S	1.000		930318
2	93056-100-013		HARNESS-ASSY:PICTURE CA S	1.000	FEATURE CONN.	920814
2	93056-620-003		HARNESS-ASSY:IDE CBL,13 S	1.000		920812
2	93056-620-004		HARNESS-ASSY:FDD CBL,34 S	1.000		920812
2	93056-740-001		HARNESS-ASSY:LED,RESET, S	1.000		920812
2	96604-703-110		HOLDER-WIRE:K106G, RICH S	1.000		930407
2	96604-703-210		HOLDER-WIRE:K103G, RICH S	1.000		920812
1#	99115-925Q001		ASSY-PACKING:SD925Q T	1.000		930318
2	90899-100-013		DRY-GEL:DESICCANT M-2 2 T	1.000	DRY	930318
2	90899-900-110		PE FILM:LDPE 0.05TX2400 T	0.083		930318
2	98114-372-007		LABEL-BARCODE:SET-BOX,1 T	2.400	BOX	930318
2	98612-914-921		PACKING-CASE:CB-SW2EGOL T	1.000		930318
2	98612-918-401		PACKING CASE,:SW-4 WHIT T	1.000		930426
2	98654-905-911		PE BAG:HDPE T0.02*150*2 T	1.000		930423
2	98704-902-050		PAD-PACKING:SW-2 YEL(SP T	1.000		930318
2	98704-904-920		PAD:PAD-MANUAL,E.P.S T	3.000	BUNDLE	930318
2	98711-908-911		CUSHION:FOAM-LEX, REV 1 T	2.000	CPU	930318
2	98794-202-110		PE BAG:HDPE+PAPER T	0.056		930318
1#	99116-50A-US1		ASSY-S/W&MNL(MSDOS) :V5 T	1.000		930318
2	94091-500-200		MS-DOS:V5.0A,ENG,3.5",S T	1.000		920603
1	99116-925-000		ASSY-USER'S GUIDE:SD925 T	1.000		930630
2	98134-925-007		MANUAL-USERS GUIDE:DESK T	1.000		930630
1#	99116-933-002		ASSY-S/W&MNL(UTY):SYSTE T	1.000		930615
2	94095-410-100		UTILITY-S/W:SYSTEM UTIL T	1.000		930508
2	94099-000-010		DISKETTE-BLANK:3.5",M-2 T	1.000		930428
2	98114-913-310		LABEL-DISKETTE:SYTEM UT T	1.000		930428
1#	99116-933-003		ASSY-S/W&MNL(UTY):VIDEO T	1.000		930615
2	94095-420-101		UTILITY-S/W:VGA UTILITY T	1.000		930508
2	94095-420-102		UTILITY-S/W:VGA UTILITY T	1.000		930508
2	94099-000-020		DISKETTE-BLANK:3.5",M-2 T	2.000		930428
2	98114-913-320		LABEL-DISKETTE:VIDEO UT T	2.000		930508
1#	99121-62M-300		ASSY-FDD(MECH):3.5" 1FD S	1.000		930318
2	96053-930-910		COVER-BLANK 5.25":EGI T S	1.000		920225
2	96613-926-110	01	BRACKET:BRKT-ASS'Y,(R)S S	1.000		920515
2	96613-926-110	02	BRACKET:BRKT-ASS'Y,(R)S S	1.000		920515
2	96613-926-120	01	BRACKET:BRKT-ASS'Y,(L)S S	1.000		920515
2	96613-926-120	02	BRACKET:BRKT-ASS'Y,(L)S S	1.000		920515
2	97088-130-062	01	SCREW-MACHINE:BH,+,M3.0 S	4.000		920225
2	97088-130-062	02	SCREW-MACHINE:BH,+,M3.0 T	4.000		920225
2	97458-230-062		SCREW-TAPTITE:BH,+S,M3. S	1.000		920225
2	97494-130-081		SCREW-TAPTITE:BH,+B,M3. T	2.000		920227

Lvl	PART NUMBER	CC	SPECIFICATION	RQTY-PER	REF DESN	DATE
2	97602-970-110		PANEL-HDD: 1VH T	1.000		920227
3	90742-185-069		RESIN-ABS:VH-0800 C7096	0.036		910220
2	98654-905-511		PE BAG:LDPE 45*50 ,REV1 T	1.000		930423
2	98654-906-010		PE BAG: ,HDPE T	1.000		920227
1#	99121-940-002		ASSY-FDD:3.5" 1.44MB,MI S	1.000		930630
2	94979-914-310		FDD:1.44MB,3.5" ,MFM S	1.000		930513
2	98114-001-050		LABEL-BARCODE:UNIT,40*7 S	1.000		920928
1#	99122-120-001		ASSY-HDD:120MB,IDE,3.5" S	1.000		930318
2	94971-935-124		HDD:127MB ,3.5" ,IDE S	1.000		930412
1	99122-7401HDD		ASSY-HDD(MECH):BRKT HDD S	1.000		930705
2	97008-106-022		SCREW-MACHINE:PH,UNC,6- S	4.000		930315
1#	99123-740-001		ASSY-SMPS:PS-103,FCC S	1.000		930318
2	94969-101-030		SMPS:PS-103 S	1.000		910916
2	97088-130-062		SCREW-MACHINE:BH,+,M3.0 S	3.000		910930
1#	99129-931-001		ASSY-SYS LABEL:UL-6L05/ T	1.000		930407
2	98114-001-030		LABEL-BARCODE:SET,55*12 T	1.000		920820
2	98114-003-010		LABEL-ID:UL-6L05/CSA-LR T	1.000		920820

Power Supply Parts List

NO	PART NUMBER	DESCRIPTION	SPECIFICATION	Q'TY	LOCATION NUMBER
1	10601-10004AT	PCB-MAIN & SUB	CEM-1, 22*190*1.6	1	S-006, S-007
2	63610-11201WA	TRANS MAIN	EER4445, TS-001	1	T1
3	63820-34301NA	LINE FILTER	TOROID	2	L1, 2
4	63808-05004CA	OUTPUT CHOCK 1	CC-025, 5uH	1	L5
5	63808-45801CA	OUTPUT CHOCK 2	CC-101, 4.5uH	1	L4
6	63808-15005QA	PEAKING-COIL	15uH, 0.23A	1	L3
7	69820-48101AA	VARISTOR(ZNR)	D62ZOV481RA80UL	1	ZNR
8	60047-00060SB	N-MOS FET	SSP6N60A, 600V6A	1	Q1
9	60016-02222PB	PNP-TRANSISTOR	MPS2222A, 40V, 0.6A	2	Q4, 6
10	60001-20907PB	PNP-TRANSISTOR	MPS2907A, 60V, 0.6A	3	Q2, 3, 5
11	62836-03842AA	IC-PWM	3842, DIPP, 8P	1	M1
12	64841-05002XA	IC-OPTO COUPLER	CQY80NG, DIP6P	1	M2
13	62841-07912JA	IC-REGULATOR	7912	1	M3
14	62841-07905JB	IC-REGULATOR	7905	1	M4
15	63440-10002SA	HB-IC	SSP-071A, 10P, SIP	1	M5
16	60212-00406RA	DIODE-BRIDGE	600V, 4A	1	D3
17	60221-00008FC	DIODE-FR	150V, 8A, TO-220	1	D13
18	60222-05402UA	DIODE-FR	200V, 3A, DO-201	1	D12
19	60221-00015RA	DIODE-FR	200V, 1.5A, DO-15	1	D5
20	60222-04007UA	DIODE-FR	1000V, 1A, DO-41	1	D2
21	60214-02545MA	DIODE-SCHOTTKY	45V, 25A, TO-220	1	D14
22	60220-04148XB	DIODE-SW	DO-35, 75V, 150mA	4	D6, 7, 9, 11
23	60211-04004DA	DIODE-GP	400V, 1A, DO-41	1	D1
24	60237-05246XA	DIODE ZENER	DO-35, 16V, 1/2W	2	D4, 8
25	60237-05250XA	DIODE ZENER	DO-35, 20V, 1/2W	1	D10
26	60232-00751XA	DIODE ZENER	DO-35, 5.1V, 1/2W	1	D15
27	69810-08001CA	THERMISTOR	8ohm, D13	1	RT1
28	60654-20280HA	VR-SEMI.	2K, 0.5W, O-TURN	1	VR1
29	60416-26155DA	RESISTOR M-F	260ohm, 1%, 1/8W	1	R46
30	60416-25255DA	RESISTOR M-F	2.49k, 1%, 1/8W	1	R21
31	60416-66155DA	RESISTOR M-F	660, 1%, 1/8W	1	R45
32	60416-50255DA	RESISTOR M-F	4.99k, 1%, 1/8W	2	R14, 20
33	60416-16355DA	RESISTOR M-F	16.2K, 1%, 1/8W	1	R16
34	60416-15355DA	RESISTOR M-F	15K, 1%, 1/8W	8	R32, 33, 34, 35, 37, 38, 39, R40
35	60416-10355DA	RESISTOR M-F	10.0K 1%, 1/8W	1	R13
36	60416-51255DA	RESISTOR M-F	5.1K, 1%, 1/8W	1	R26
37	60401-10075HA	RESISTOR CRN	10ohm, 5%, 1/2W	2	R29, 42
38	60401-39175HA	RESISTOR CRN	390ohm, 5%, 1/2W	1	R41
39	60401-30075DA	RESISTOR CRN	30ohm, 5%, 1/8W	1	R10
40	60401-10175DA	RESISTOR CRN	100ohm, 5%, 1/8W	1	R19
41	60401-12175FA	RESISTOR CRN	120ohm, 5%, 1/4W	1	R28
42	60401-10275DA	RESISTOR CRN	1K, 5%, 1/8W	2	R9, 17
43	60401-20275DA	RESISTOR CRN	2K, 5%, 1/8W	2	R22, 25
44	60401-20275FA	RESISTOR CRN	2K, 5%, 1/4W	1	R23
45	60401-33275FA	RESISTOR CRN	3.3K, 5%, 1/4W	1	R11
46	60401-36275FA	RESISTOR CRN	3.6K, 5%, 1/4W	1	R24
47	60401-36275DA	RESISTOR CRN	3.6K, 5%, 1/8W	1	R18
48	60401-10375DA	RESISTOR CARBON	10K, 5%, 1/8W	2	R8, 15
49	60401-30375FA	RESISTOR CARBON	30K, 5%, 1/4W	1	R43
50	60401-47475HA	RESISTOR CARBON	470K, 5%, 1/2W	1	R1
51	60442-03852LA	RESISTOR W/W	0.3ohm, 1%, ARW N1W	1	R7

NO	PART NUMBER	DESCRIPTION	SPECIFICATION	Q'TY	LOCATION NUMBER
52	60421-22172NA	RESISTOR MOR	220ohm, 5%, 2W	1	R44
53	60455-10379TA	RESISTOR CEMENT	10K, 5%, 5W	1	R4
54	60421-10372QA	RESISTOR MOR	10K, 5%, 3W	2	R6, 36
55	60421-20272QB	RESISTOR MOR FP	2K, 5%, 3W	1	R5
56	60421-10472LA	RESISTOR MOR	100K, 5%, 1W	2	R2, 3
57	60421-15172NA	RESISTOR MOR	150ohm, 5%, 2W	1	R27
58	60821-10327ZZ	CERAMIC CAP	CK, 0.01uF, 500VZ5U	2	C41, 42
59*	60826-22130KB	CERAMIC CAP	220P 1KV, K	1	C11
60+	60826-10130KB	CERAMIC CAP	100P 1KV, K	1	C11
61	61266-22330KA	MF-CAP	0.022uF 1KVDC	1	C10
62	60920-10217MA	M-L CERAMIC	1000P 50VDC, X7R	1	C24
63	60920-22217MA	M-L CERAMIC	2200P 50VDC, X7R	1	C16
64	60920-22317MA	M-L CERAMIC	0.022uF 50VDC, X7R	1	C15
65	60920-10417MD	M-L CERAMIC	0.1uF 50VDC, Z5U	13	C14, 17, 18, 19, 20, 22, 23, C28, 29, 33, 37, 48, 50
66	61215-10320KB	FOLY FILM CAP	0.01uF, 100VDC, 5%	1	C51
67	61215-10220TA	FOLY FILM CAP	1000P, 100VDC, 5%	2	C45, 46
68	61412-33124MA	AL-ELEC CAP	SMS-250V-330uF-M	2	C8, 9
69	61414-39210MA	AL-ELEC CAP	STL-10V-3900uF-M	2	C34, 35
70	61414-10212MP	AL-ELEC CAP	ST-25V-1000-M	1	C30
71	61414-68112MC	AL-ELEC CAP	STL-16V-680-M	1	C32
72	61414-10210MH	AL-ELEC CAP	STL-10V-1000uF-M	1	C36
73	61414-47114MF	AL-ELEC CAP	ST-25V-470uF-M	2	C25, 31
74	61414-47017MF	AL-ELEC CAP	GLT-50V-47uF-M	1	C13
75	61414-22114MG	AL-ELEC CAP	ST-25V-220uF-M	1	C26
76	61414-10110MB	AL-ELEC CAP	GLT-10V-100uF-M	1	C27
77	61414-10017MP	AL-ELEC CAP	GLT-50V-10uF-M	3	C12, 43, 49
78	61414-47817MK	AL-ELEC CAP	GLT-50V-4.7uF-M	2	C21, 47
79	60826-10230KB	CERAMIC CAP	1000PF, 1KV, K	1	C44
80	71835-05021BA	VOLT. SEL. S/W ASS'Y	L60mm, S2	1	CASE
81*	71807-05012CA	IN LET ASS'Y	L145mm, S3	1	CASE
82+	71807-05012CB	IN LET ASS'Y	L145mm, S3	1	CASE
83	71836-05006BA	FAN ASS'Y	L145mm, S2	1	CASE
84	71801-05076VA	DC OUTPUT ASS'Y	L270mm, S20	1	MAIN PCB
85	71808-05050BA	WIRE-ASS'Y	L110mm, S2	1	MAIN to SUB
86	70213-80010AA	CONNECTOR-WAFER	5045-02A SR 2.5WHT	1	CON4
87	70213-20006AA	CONNECTOR-WAFER	5096-02C, SR3.96 2P	2	CON1, 3
88	10611-07004NA	CASE COVER	122.2*150*74*1.0t	1	SET ASS'Y
89	10612-10003NA	CASE BOTTOM	120*150*75*1.0t	1	SET ASS'Y
90	10610-35400EA	HEAT SINK-1	FET	1	HS1
91	10610-35460AA	HEAT SINK-2	DIODE	1	HS2
92	10610-51020SA	HEAT SINK-3	REGULATOR	1	HS3
93	10616-11300PA	CLAMP-TR, TO-220	GLASS-FILLED NYLON	1	FET(Q1)
94	10616-22300BA	CLAMP-TR	#8, SECC, ZN-W, T1.0	1	D13, 14
95	50862-03022EA	NUT	HEX m3*2.2 ZPS(YEL)	4	FET, HS3, V/S
96	50862-04032EA	NUT	HEX M4*3.2	1	F/G
97	50232-30069EA	SCREW	TAPTITE PH+M3*6	2	CASE+BOTTOM
98	50052-40121NA	SCREW	MACHINE PH+M4*12	1	F/G
99	50438-30082EA	SCREW	MACHINE PH+M3*8 NI	1	SUB PCB
100	50032-30101EA	SCREW	MACHINE PH+M3*10	1	HS2
101	50438-30081EA	SCREW	SPECIAL PH+SW+M3*8	4	PCB, S/W
102	50052-30321NA	SCREW	MACHINE TH+M3*32	4	FAN
103	50438-30121EA	SCREW	SPECIAL PH+SWM3*12	2	FET, M3. M4
104	51072-04004EA	WASHER-START	TOH-EX I4 R8.5	1	F/G

NO	PART NUMBER	DESCRIPTION	SPECIFICATION	Q'TY	LOCATION NUMBER
105	51022-03007EA	WASHER-SPRING	I3, R5, T0.7	2	V/S
106	51022-04010EA	WASHER-SPRING	I4, R7, T1.0	1	F/G
107	70010-04005WA	POWER SWITCH, PB	5A 250VAC, 2POLE	1	SW1
108	70840-00001AA	INLET	250VAC10A 42RO3	1	CASE
109	70068-06007WA	VOLT. SELECTOR SW	250VAC5A SE-1022	1	CASE
110	71431-13001FA	MAGNET-FRIT	5943000301	1	OUT CABLE
111	59852-00003AA	GROMMENT	I17, R22, BLACK	1	OUT CABEL
112	83220-50016AA	MOTOR-DC, FAN	12VDC, 0.08A, 60*60	1	BOTTOM
113	10641-09004AA	SER NO LABEL		1	CASE
114	83235-10012AA	ADJ LABEL	+5V	1	CASE
115	83235-10013AA	INSPECTED LABEL		1	CASE
116*	83220-50017ZZ	INDICATOR	RATING LABEL	1	COVER
117+	83220-50017AC	INDICATOR	RATING LABEL	1	COVER
118*	01276-47424MA	CAPACITOR-X	0.47uF 250VAC	1	C1
119	01277-22424MA	CAPACITOR-X	0.22uF 250VAC	1	C2
120*	61267-10424MA	CAPACITOR-X	0.1uF 25VAC	1	C53
121+	01276-47424MA	CAPACITOR-X	0.47uF 250VAC	1	C53
122	60830-33224MA	CAPACITOR-Y	3300pF, 250VAC	2	C39, 40
123*	60830-33224MA	CAPACITOR-Y	3300pF, 250VAC	6	C3, 4, 5, 6, 7, 52
124+	60830-22224MA	CAPACITOR-Y	2200pF, 250VAC	4	C3, 4, 6, 7
125+		JUMPER WIRE	10mm, D0.6	2	C5, 52
126*	71030-59002BA	FUSE POWER	3A, 250V, 5.2*20	1	F1
127+	71030-60004DA	FUSE POWER	3.15A, 250V	1	F1
128	79822-18001LA	FUSE CLIP	5A, L23, AUTO	2	F1
129	10622-18009HA	INSULATOR	SILICON 25*37	1	HS2(D13, 14)
130	10622-07002JA	INSULATOR	PVC, T0.5, 102*70	1	BOTTOM
131	10621-16001GA	INSULATOR 1	SILICON 13*18	2	HS3(M3, M4)
132	10622-18008HA	INSULATOR 2	SILICON 25*29	1	HS1(Q1)
133	10622-30001WA	INSULATOR-RING	PVC	2	HS3(M3, M4)
134	10615-12001NA	FAN PLATE	#60	1	CASE
135	79820-00001AA	FAN, GRILL-ROUND	60*60	1	CASE

Appendix. The Local Super VGA

1. Quick Installation Guide for Cirrus Windows 3.1 Device Driver

Setting Flows of Cirrus High-Resolution Video Mode in Windows 3.1

1). Start Windows.

2). In the program manager, choose Windows Setup.

3). Install Cirrus's Windows 3.1 Device Driver program on new directory.
ex.: c:\windows\cirrus
(After install, "SETRES" icon will be displayed on Windows screen.)

4). Exit Windows. (or select "DOS prompt" icon.)

5). Examine your monitor's Resolution Capability.

6). Execute "CLMODE.EXE" on DOS prompt, to enroll your monitor's Resolution mode.
(After this step "SETRES" icon in Windows will be operate properly.)

7). Exit "CLMODE.EXE" screen with "ESC" key, and save the settings or not.

8). Restart Windows and select "SETRES" icon to select Resolutions and Colors.
(or Exit "DOS prompt" mode on Windows.)

9). Select Resolutions and colors.

10). Restart Windows.

11). Selected Resolutions and Colors will be displayed.

*** Resolutions and Colors are restricted by your monitors. ***

2. VGA Modes

The Cirrus Logic VGA BIOS supports all standard VGA modes. These standard VGA modes are listed in the following Table 1.

Table 1. Standard VGA Modes

Mode #,	VESA Mode #	# of Colors	Char. x Row	Char Cell	Pixels	Display Mode	Horiz Freq. (kHz)	Vert. Freq. (Hz)
11/01	—	16/256	40x25	8x8	320x200	Text	31.5	70
00*/01*	—	16/256	40x25	8x14	320x350	Text	31.5	70
00**/01**	—	16/256	40x25	9x16	360x400	Text	31.5	70
02*/03*	—	16/256	80x25	8x8	640x200	Text	31.5	70
02**/03**	—	16/256	80x25	8x14	640x350	Text	31.5	70
02/03	—	16/256	80x25	9x16	720x400	Text	31.5	70
04/05	—	4/256	40x25	8x8	320x200	Graphics	31.5	70
06	—	2/256	80x25	8x8	640x200	Graphics	31.5	70
07*	—	mono	80x25	9x14	720x350	Text	31.5	70
07**	—	mono	80x25	9x16	720x400	Text	31.5	70
0D	—	16/256	40x25	8x8	320x200	Graphics	31.5	70
0E	—	16/256	80x25	8x8	640x200	Graphics	31.5	70
0F	—	mono	80x25	8x14	640x350	Graphics	31.5	70
10	—	16/256	80x25	8x14	640x350	Graphics	31.5	70
11	—	2/256	80x30	8x16	640x480	Graphics	31.5	60
12	—	16/256	80x30,	8x16	640x480	Graphics	31.5	60
13	—	256/256	40x25,	8x8	320x200	Graphics	31.5	70

Note) * : EGA, ** : VGA

The Cirrus Logic GD540X,542X VGA BIOS supports standard VESA and extended modes. These modes are listed in the following Table 2.

Table 2. Standard VESA and Extended Modes

Mode #,	VESA	# of Colors	Char.x Row	Char. Cel	Screen Format	Display Mode	Dot Clock MHz	Horiz. Freq. (kHz)	Vert. Freq. (Hz)
14	—	16/256K	132x25	8x16	1056x400	Text	41.5	31.5	70
54	10A	16/256K	132x43	8x8	1056x350	Text	41.5	31.5	70
55	109	16/256K	132x25	8x14	1056x350	Text	41.5	31.5	70
58,6A	102	16/256K	100x37	8x16	800x600	Graphics	36	35.2	56
58,6A	102	16/256K	100x37	8x16	800x600	Graphics	40	37.8	60
58,6A	102	16/256K	100x37	8x16	800x600	Graphics	50	48.1	72
5C	103	256/256K	100x37	8x16	800x600	Graphics	36	35.2	56
5C	103	256/256K	100x37	8x16	800x600	Graphics	40	37.9	60
5C	103	256/256K	100x37	8x16	800x600	Graphics	50	48.1	72
5Di	104	16/256K	128x48	8x16	1024x768	Graphics	44.9	35.5	87i
5D	104	16/256K	128x48	8x16	1024x768	Graphics	65	48.3	60
5D	104	16/256K	128x48	8x16	1024x768	Graphics	75	56	70
5D	104	16/256K	128x48	8x16	1024x768	Graphics	77	58	72
5F	101	256/256K	80x30	8x16	640x480	Graphics	25	31.5	60
5F	101	256/256K	80x30	8x16	640x480	Graphics	31.5	37.9	72
60i	105	256/256K	128x48	8x16	1024x768	Graphics	44.9	35.5	87i**
60	105	256/256K	128x48	8x16	1024x768	Graphics	65	48.3	60
60	105	256/256K	128x48	8x16	1024x768	Graphics	75	56	70
60	105	256/256K	128x48	8x16	1024x768	Graphics	77	58	72
64	111	64K/64K	—	—	640x480	Graphics	25	31.5	60
64	111	64K/64K	—	—	640x480	Graphics	62.8	37.9	72
65	114	64K/64K	—	—	800x600	Graphics	72	35.2	56
65	114	64K/64K	—	—	800x600	Graphics	80	37.8	60
66	110	32K/32K*	—	—	640x480	Graphics	25	31.5	60
66	110	32K/32K*	—	—	640x480	Graphics	62.8	37.9	72
67	113	32K/32K*	—	—	800x600	Graphics	72	31.5	56
6Ci	106	16/256K	160x64	8x16	1280x1024	Graphics	75	48	87i**
6F	10E	64K/64K	40x25	8x8	320x200	Graphics	25	31.5	70
70	10F	16M/16M	40x25	8x8	320x200	Graphics	37.7	31.5	70
70i	112	16M/16M	80x30	8x16	640x480	Graphics	75.5	31.5	60

Note : *) 32K direct color/256 color mixed mode
**) A character "i" stands for interlaced mode

3. VGA Utility Software

Several utility programs are supplied with your Cirrus Logic VGA. The following section describes these utilities and how to use them.

Clmode is a program supplied with your Cirrus Logic VGA to configure it's various options.

SetRES lets the user change the operating resolution and the number of colors from within Windows.

1) Clmode

The Clmode utility allows the user to define the type of monitor attached and set the video modes supported by the Cirrus Logic VGA.

- Using Clmode's menu-driven interface

At the DOS prompt type:

CLMODE [Enter]

The main popup window consists of a number of buttons. Each button represents a different option or menu. The underlined letter of a button name specifies the hot key combination for that item. For example, press the [Alt] and the underlined letter keys simultaneously or just the underlined letter key to select an option. Note if you intend to use a mouse with Clmode, then a mouse driver should first be installed prior to running the Clmode utility.

- Choosing the attached monitor type

Selecting the proper monitor type will allow the Cirrus Logic VGA to display the highest quality output that it is capable of with the attached monitor. The monitor type determines what video modes will be available to your system. It will also determine the vertical refresh rates available. Generally, the higher the refresh, the better the screen will look. A description of the available monitor types is given in Table D-3 at the end of this section.

The high refresh option of Clmode allows the user to force some video modes to a higher refresh rate. The option will not work on some monitors.
If high refresh is selected, the user must verify that the connected monitor can support the option by using Clmode from the command line to set video mode 12 . If any problems are observed, disable the option by typing CLMODE 3 m-[Enter] from the directory containing CLMODE.EXE.

Select the Monitor Type button. The Monitor Type setup window will be displayed. The current monitor type and refresh rate will be highlighted initially. Use the keyboard or the mouse to choose the type of monitor attached. To move down to the Refresh Rate selection box, use the mouse or press the [Tab] key. Press the Save button to set the new monitor type. Press the Cancel button to discard any changes. Press the Help button to get a detailed explanation on the monitor types and the VGA refresh rates.

On some systems the monitor type will be remembered from one session to the next. To test this, select a monitor type and exit the Clmode program. Turn the computer off for ten seconds. After rebooting the computer, run Clmode and verify whether or not the monitor that you selected is zstill enabled. If it is, it should not ever need to be set again in normal use. If the monitor type was not kept then you should select the option to have Clmode save the monitor type in you AUTOEXEC.BAT file. You will be given this choice after selecting the Save button.

- Available video modes

Select the Video Mode button. The Video Mode Setup window displays all the modes supported according to the monitor type attached and the amount of video memory present. This list of video modes will tell you which are available in your current configuration for use with extended resolution drivers.

- Retrieving the current VGA controller status

The information in the main window displays the VGA controller type, the BIOS version number and the amount of video memory present.

- Getting help

Clmode provides Help for the following items: Monitor Type, Video Modes, Mouse, Keyboard and About Clmode. The Monitor Type help window explains the different capabilities of each monitor type.

The Video Mode help window defines the information given in the Video Mode window. The Keyboard and Mouse help windows explain how to use the keyboard and the mouse to make selections. The About window displays the Cirrus Logic copyright message and the Clmode version number.

- Exiting the Clmode

To exit Clmode at any time, press [Alt] and [F4] keys simultaneously, or click the left mouse button on the system button of the main window (i.e. The top left corner button of the window which is shown as a dot), or select the Exit button. When the Clmode utility exits, the current video mode, monitor type, and VGA refresh rate will be displayed.

- Using Clmode's command line options

When command line options for CLMODE.EXE are given at the DOS prompt, the menu-driven windows will not be displayed. Instead, monitor type, video mode and refresh rate will be set at the DOS prompt. The command line options for CLMODE.EXE are:

CLMODE [[modenum][+*-]] [m[montype][refresh]]
[modenum] mode number
[+*-]+ selects 400 lines (default)
* selects 350 lines
- selects 200 lines
[montype] monitor type
[refresh]high or low VGA refresh rate (+ or -)

For example, to select mode 3 with high VGA refresh for a Super VGA monitor, type the following command at the DOS prompt:
CLMODE 3+ m2+ [Enter]

Typing an invalid option will display the command line help text. Typing [S] as a command line option will display the current Clmode settings.

Following is a table of common monitor types. Resolutions with more then one entry per line in the vertical frequency column signify the availability of the high refresh option.

Table 3. Monitor Type Examples

Monitor Type	Examples		Horizontal Freq (kHz)	Vertical Freq (Hz)	Display Resolution
	SAMSUNG	Others			
0	CVl4951 CLV4955	IBM 8512, 8513 8503	31.5	60 or 70	640x480
1	SyncMaster 2 SyncMaster 3	IBM 8514, 8515	31.5 35.5	60 or 70 43.5 - interlaced	640x480 1024x768
2	SyncMaster 3N SyncMaster 15C	NEC 2A	31.5 35.2	60 or 70 56	640x480 800x600
3		NEC II	31.5 35.2 35.5	60 or 70 56 43.5 - interlaced	640x480 800x600 1024x768
4		NEC 3D	31.5 37.8 37.8	60 or 70 60 43.5 - interlaced	640x480 800x600 1024x768
5		Sony CPD-1304, NEC 3FGx, Nanao 9065S, 9070U	31.5 48.0 48.0 48.0	60 or 70 72 60 43.5 - interlaced	640x480 800x600 1024x768 1280x1024
6		NEC 4D, 4FG, Nanao T240i	31.5 48.0 56.0 48.0	60 or 70 72 70 43.5-interlaced	640x480 800x600 1024x768 1280x1024
7	SyncMaster 5C SyncMaster 6C SyncMaster 7C	NEC 5D 5FG, 6FG Nanao T550i, T660i, F550i, F750i	31.5 48.0 58.3 48.0	60 or 70 72 72 43.5 - interlaced	640x480 800x600 1024x768 1280x1024

2) SetRES

SetRES is a utility that runs under Windows 3.x. It allows the user to change the screen resolution, number of screen colors, and select either large or normal fonts and system resources.

After new options have been selected, the user can either immediately restart Windows, in which case the new resolution will take effect immediately, or continue working in the current resolution, in which case the new resolution will take effect the next time Windows is started. Note that under Windows 3.0 large and normal font selection is not allowed.

This application assumes that the Windows drivers have been correctly configured using Windows Setup. For information on installing and configuring Windows display drivers using setup, please refer to the Microsoft Windows section in this manual. From Windows Setup select the Multi-Resolution entry. This will correctly configure the driver for Windows 386 enhanced mode operation, and copy the necessary font files to your hard disk.

〉Installation

1) Start Windows.

2) In the Program Manager, choose File Run.

   Specify the diskette drive where the Windows Drivers and Utilities Diskettinserted, and run the install program. For instance if the floppy is in drive A:, type

   A:\INSTALL〈D〉[Enter]

3) When prompted, specify to copy the files to the Windows directory.

   SetRES may now be run by selecting the SetRES icon.
   Use the SetRES utility to select supported colors and resolutions.

   If your are unsure what resolutions and colors your video card can support, refer to the Section of this manual on Clmode for information on how to determine supported resolutions.

   For help on the SetRES utility, select Help from the program menu.

4. Display Drivers

The Cirrus Logic video controller is 100% VGA compatible. The display drivers described in this manual are supplied to improve the resolution for each supported software application package.

It can support improved text resolution, providing greater readability when using the supplied drivers in text-based word processing programs It also supports higher graphics resolutions, providing greater detail when using the supplied drivers in graphics-based programs.

In each application section, there will be a brief introduction describingthe application and the revision level of the application supportedby the supplied display drivers.

The installation instructions for each display driver will followthe introduction section. Follow the instructions carefully to besure that each display driver is correctly installed. All of the installation instructions assume that the Cirrus Logic Drivers Diskette is located in drive A:. If drive B: is used, the instructions should changedappropriately.

The installation utility (INSTALL.EXE) should be used to copy display drivers directly to the appropriate application directories where they may be configured by the application software.

〉 Before you begin

It is assumed that the user is familiar with DOS and certain DOS commands.
Please review the installation instructions and the associated DOScommands before attempting the actual installation.

Not all video modes will be available on all systems. If an extendedmode driver is installed for a video mode that is not available, the application program will not function properly. There are a number of things that determine the list of available video modes. Some of these include the current monitor type, the amount of installed memory, and the revision of the VGA controller. To determine which modes areavailable before beginning the driver installation, it is recommendedthat the user run the Clmode program and examine the list of availablevideo modes.

5. Microsoft Windows

- Installing Windows 3.1 display drivers

To install the Windows 3.1 drivers from the DOS prompt, proceed as follows:

1) Insure that Windows 3.1 is already installed on your computer.

2) From your Windows directory, at the DOS prompt, type SETUP[Enter] to run the Windows SETUP.EXE program. Follow the instructions on the screen. When you come to the screen which lists the hardware and software components such as display adapter (e.g. VGA, CGA, etc.), keyboard type, mouse type, etc., go to the Display selection by using cursor keys to move the highlighted bar and press [Enter].

3) From the next menu listing of display options, scroll to the bottom of the list, and highlight the following text:

Other (Requires disk provided by a hardware manufacturer)

Press [Enter], and when prompted, insert the Windows Display Driver diskette into drive A: and type<B> A:\<D>[Enter].
4) You will see the list of drivers and their associated resolutions.

5) Highlight the desired choice by moving the cursor to the correct display driver, and then press [Enter].

6) Continue with the remainder of the setup procedure.

To install the Windows 3.1 drivers from within Windows, proceed as follows:

1) Insure that Windows 3.1 is already installed on your computer andstart Windows.

2) From the Main window of the Program Manager run the Windows 3.1Setup program.

3) Select Change Systems Settings... from the Options menu of Setup.

4) Click on the down arrow at the right side of the Display: line.Scroll to the end of the list of available display drivers and select Other display (Requires disk from OEM)....

5) Insert the Windows display driver diskette into drive A: and type A:\[Enter] as the pathname, then click on OK.

6) You will see the list of available drivers and their associated resolutions.

7) Highlight by moving the cursor to the desired display driver, and then click on OK.

8) Continue with the remainder of the setup procedure. The changes will not take effect until Windows is restarted.

© SAMSUNG Electronics Co., Ltd. 1993
98134-925-009
Rev. 1.0
Printed in Korea